

S5D2400X

Data Sheet

Revision 0.0



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1 OVERVIEW

1.1 OVERVIEW

S5D2400X scaling image processor is a display SOC designed for TFT-LCD monitors and TV systems. This chip consists of Scaler, Deinterlace and ACE block. The chip receives the signal of digital RGB 24-bit or ITU-R BT.656/601 format, deinterlaces the signal and sends the single or dual channel digital data (24-bit or 48-bit). The chip provides the ACCE (Adaptive Color & Contrast Enhancement) function that minimizes color change and improves brightness function, and has the built-in filter that improves sharpness. The built-in OSD supports 512 ROM fonts of 12*18 matrix, and processes 28 RAM fonts.

1.2 APPLICATIONS

- Multimedia LCD Monitors/TVs
- Digital TVs
- CRTs and Rear Projection TVs
- Plasma Displays
- Projection Displays

1.3 FEATURES

- **High-Quality Advanced Scaling**
 - Fully Programmable Scale-Up Ratios
 - Scale-up or down for Horizontal and Vertical
- **Built-in OSD for LCD Monitor**
 - 512 ROM Fonts
 - 28 RAM Fonts
- **Economic Output Clock Source**
 - Built-In PLL Core
 - External X-tal Device
- **Supports I²C Bus Host Interface**
- **R/G/B Gamma look-up table**
- **Dithering**
 - 8 to 6 Dithering

- **Color & Contrast Management**
 - Adaptive Contrast Control
 - Adaptive Brightness Control
 - Image Sharpness Control
 - Color Compensation
 - Boost Up Sub Zone

- **Digital RGB input**
- **Video De-interlacing**
 - ITU-R BT.656 Interfacing
 - ITU-R BT.601 Interfacing
 - Spatial Interpolation Filter

- **PKG Information**
 - PKG: 100-TQFP-1414 (100TQFP)

- **Operating Conditions**
 - 1.8 Volts Core
 - 3.3 Volts I/O

2 PIN INFORMATION

2.1 PIN CONFIGURATION

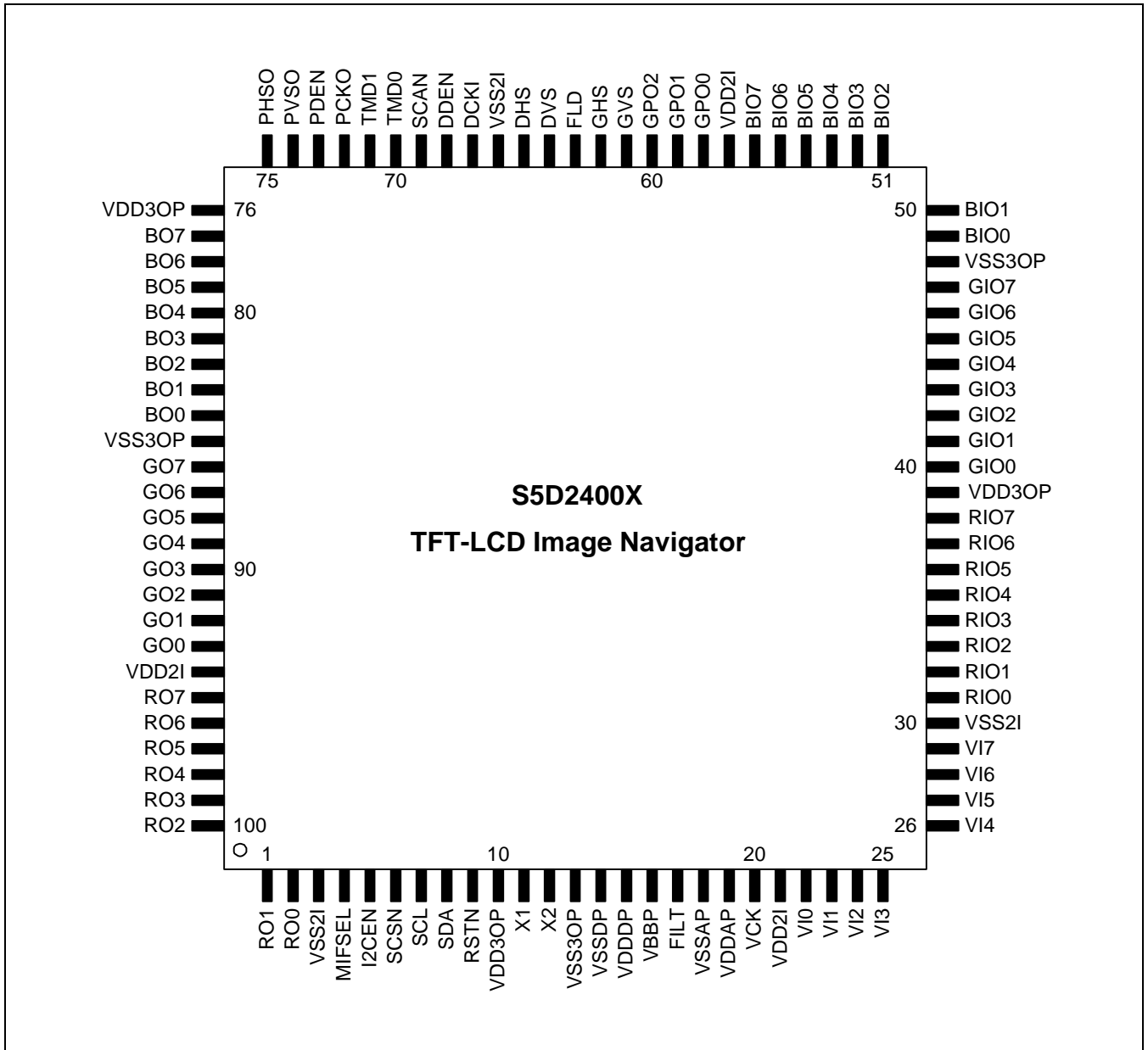


Figure 1. S5D2400X Pin Configuration

2.2 PIN DESCRIPTION

I/O Legend : I = Input O = Output P = Power G = Ground

Table 1. MCU Interface Pins

Pin Name	I/O	Pin No	Description
MIFSEL	I	4	MCU I/F Logic Selection (Always High)
I2CEN	I	5	I ² C Enable Signal (Always High)
SCSN	I	6	Chip Select Signal. (Always High)
SCL	I	7	Serial Bus Clock
SDA	I/O	8	Serial Bus Data (I: Input Data, O: Output Data)
GPO0	O	58	General Purpose Output 0
GPO1	O	59	General Purpose Output 1
GPO2	O	60	General Purpose Output 2

Table 2. PLL Interface Pins

Pin Name	I/O	Pin No	Description
X1	I	11	X-tal Input (Max 30 MHz)
X2	O	12	X-tal Output
FILT	O	17	PLL External Loop Filter (Refer to the circuit diagram on Page 14.)

Table 3. Video Input Interface Pins

Pin Name	I/O	Pin No	Description
VCK	I	20	Input Clock for Video Mode (De-Interlace)
VI[7:0]	I	22~29	ITU-R BT.656: Video Data Input Port ITU-R BT.601: Y Data Input Port Pull down by internal 70kΩ resistors
GVS	I	61	ITU-R BT.601: V-SYNC Input from Decoder
GHS	I	62	ITU-R BT.601: H-SYNC Input from Decoder
FLD	I	63	ITU-R BT.601: External FIELD Signal Input

Table 4. DVI Interface Pins

Pin Name	I/O	Pin No	Description
RSTN	I	9	System Reset (Low Active)
RIO[7:0]	I/O	31 ~ 38	Input or Dual Output Port RED[7:0] ITU-R BT.601: UV Data Input Port Pull down resistors
GIO[7:0]	I/O	40 ~ 47	Input or Dual Output Port GREEN[7:0] Pull down resistors
BIO[7:0]	I/O	49 ~ 56	Input or Dual Output Port BLUE[7:0] Pull down resistors
DVS	I	64	V-SYNC Input
DHS	I	65	H-SYNC Input
DCK	I	67	Input Clock
DDEN	I	68	Input Data Enable (Digital Input Mode)

Table 5. Panel Interface Pins

Pin Name	I/O	Pin No	Description
RO[7:0]	O	1~2 95~100	Single Output Port RED[7:0]
PCKO	O	72	Output Clock
PDEN	O	73	Output Data Enable
PVSO	O	74	V-SYNC Output
PHSO	O	75	H-SYNC Output
BO[7:0]	O	77~84	Single Output Port BLUE[7:0]
GO[7:0]	O	86~93	Single Output Port GREEN[7:0]

Table 6. Test Pins

Pin Name	I/O	Pin No	Description
SCAN	I	69	Scan Enable Signal for test. Not use normal condition (Always Low)
TMD0	I	70	Test Mode Selection 0 (Always Low)
TMD1	I	71	Test Mode Selection 1 (Always Low)

Table 7. Supply Voltage and Ground Pins: 3.3 / 1.8 Volt

Pin Name	Pin Number	Description
VSS2I	3, 30, 66	Internal ground
VDD3OP	10, 39, 76	3.3V Output-Driver and Pre-Driver supply voltage
VSS3OP	13, 48, 85	Output-Driver and Pre-Driver ground
VSSDP	14	PLL Digital ground
VDDDP	15	1.8V PLL Digital supply voltage
VBBP	16	PLL Bulk-Bias ground
VSSAP	18	PLL Analog ground
VDDAP	19	1.8V PLL Analog supply voltage
VDD2I	21, 57, 94	1.8V Internal Supply voltage

Total Supply Voltage : 8 Pin (3.3V: 3 Pin, 1.8V: 3 Pin, PLL (1.8V): 2 Pin)

Ground : 9 Pin (3.3V: 3 Pin, 1.8V: 3 Pin, PLL (1.8V): 2 Pin, Analog (Bulk-Bias 1.8V): 1 Pin)

3 FUNCTIONAL BLOCK DIAGRAM

3.1 SYSTEM BLOCK DIAGRAM

— ITU-R BT.656 Input to Single RGB Output System

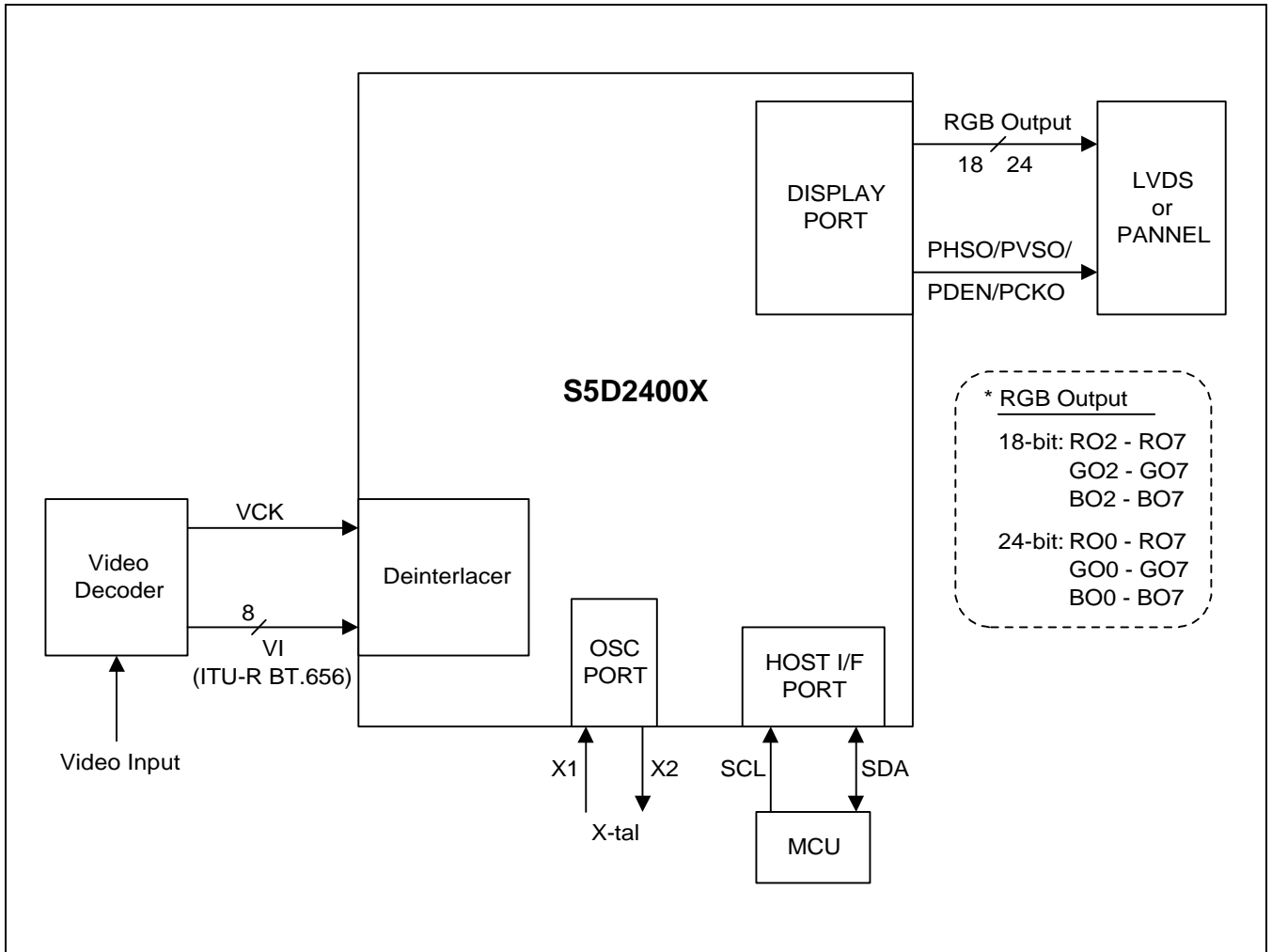


Figure 2. S5D2400X System Block Diagram (ITU-R BT.656 Input to Single RGB Output)

— ITU-R BT.656 Input to Dual RGB Output System

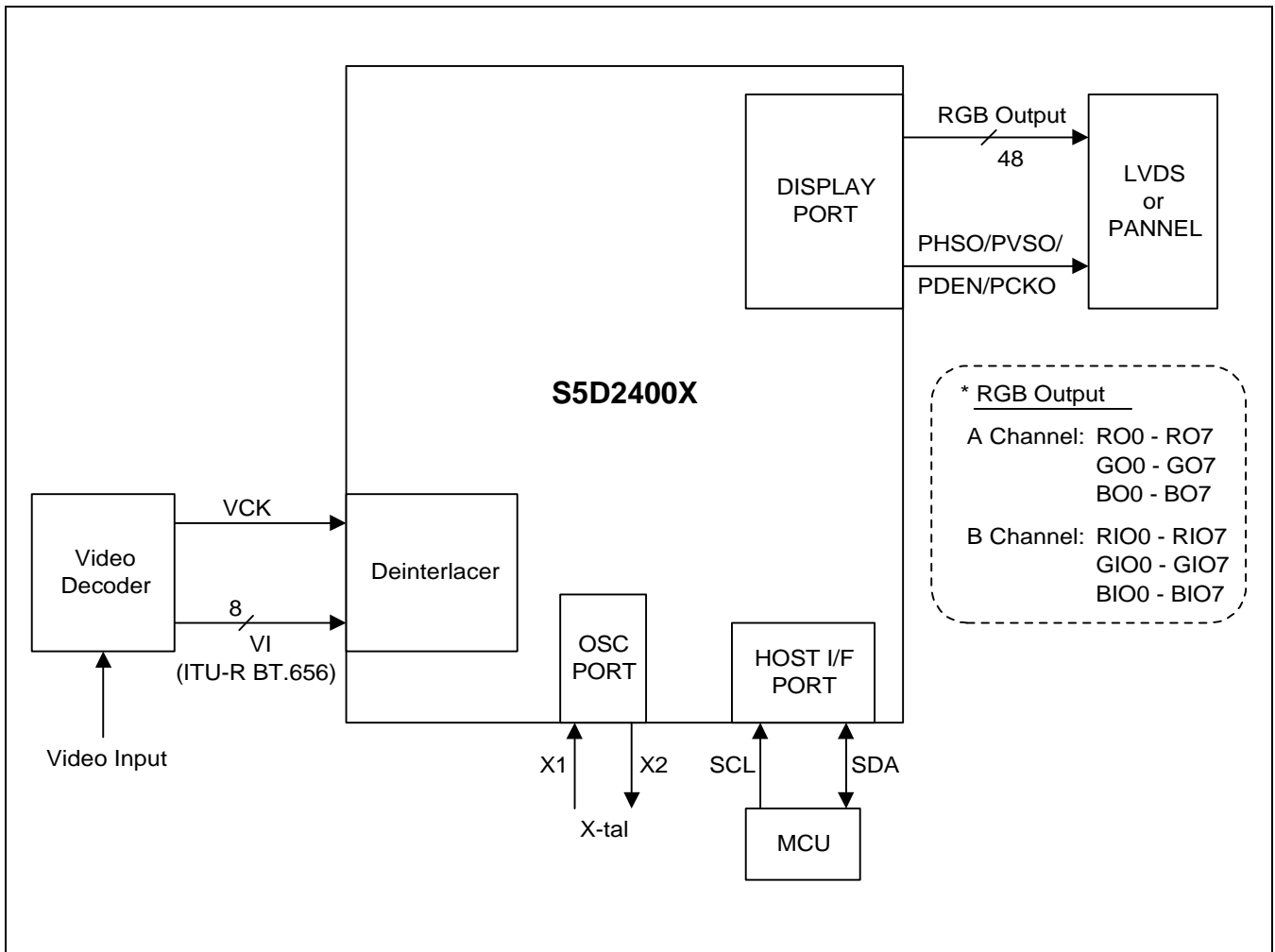


Figure 3. S5D2400X System Block Diagram (ITU-R BT.656 Input to Dual RGB Output)

— ITU-R BT.601 Input to Single RGB Output System

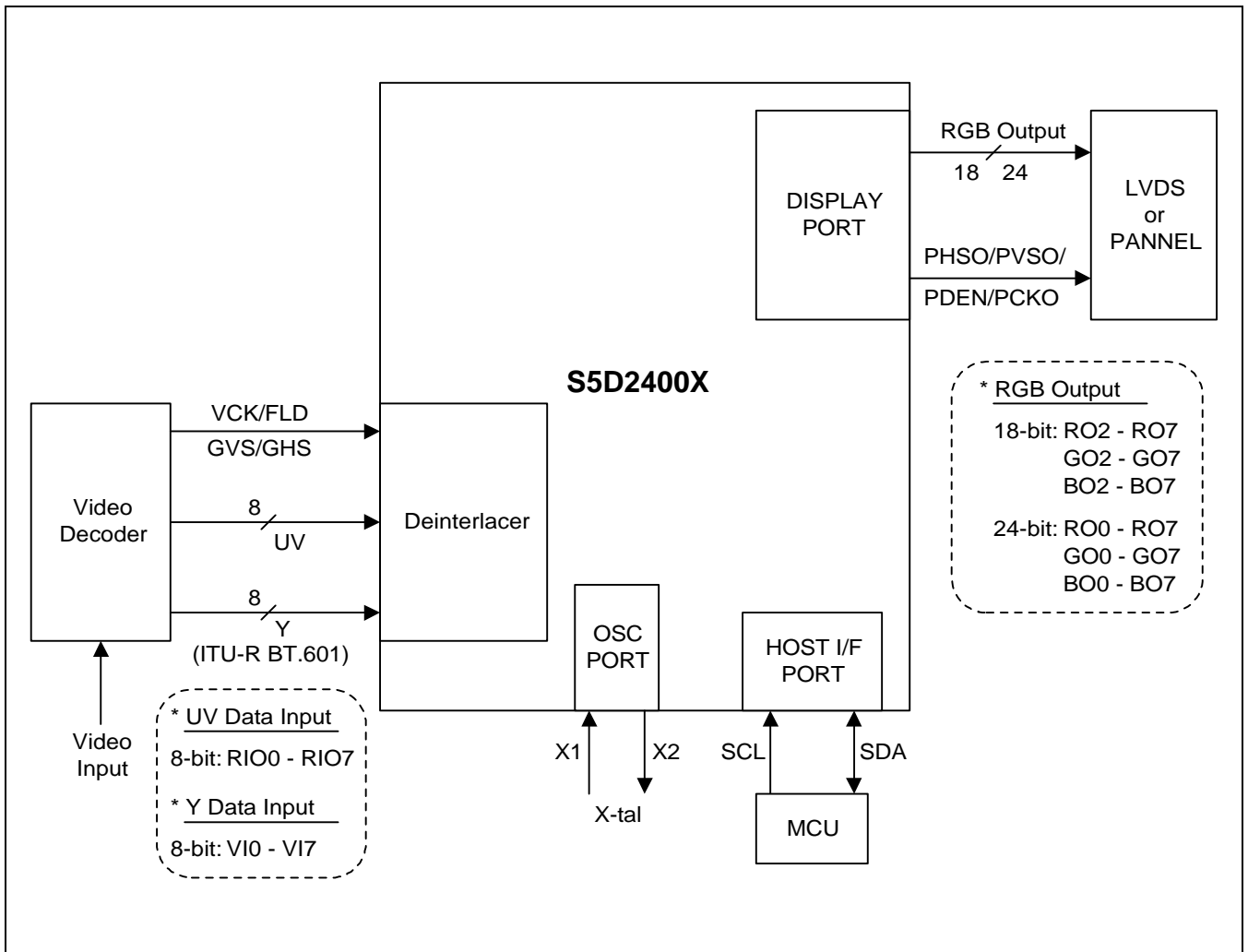


Figure 4. S5D2400X System Block Diagram (ITU-R BT.601 Input to Single RGB Output)

— DVI Input to Single RGB Output System

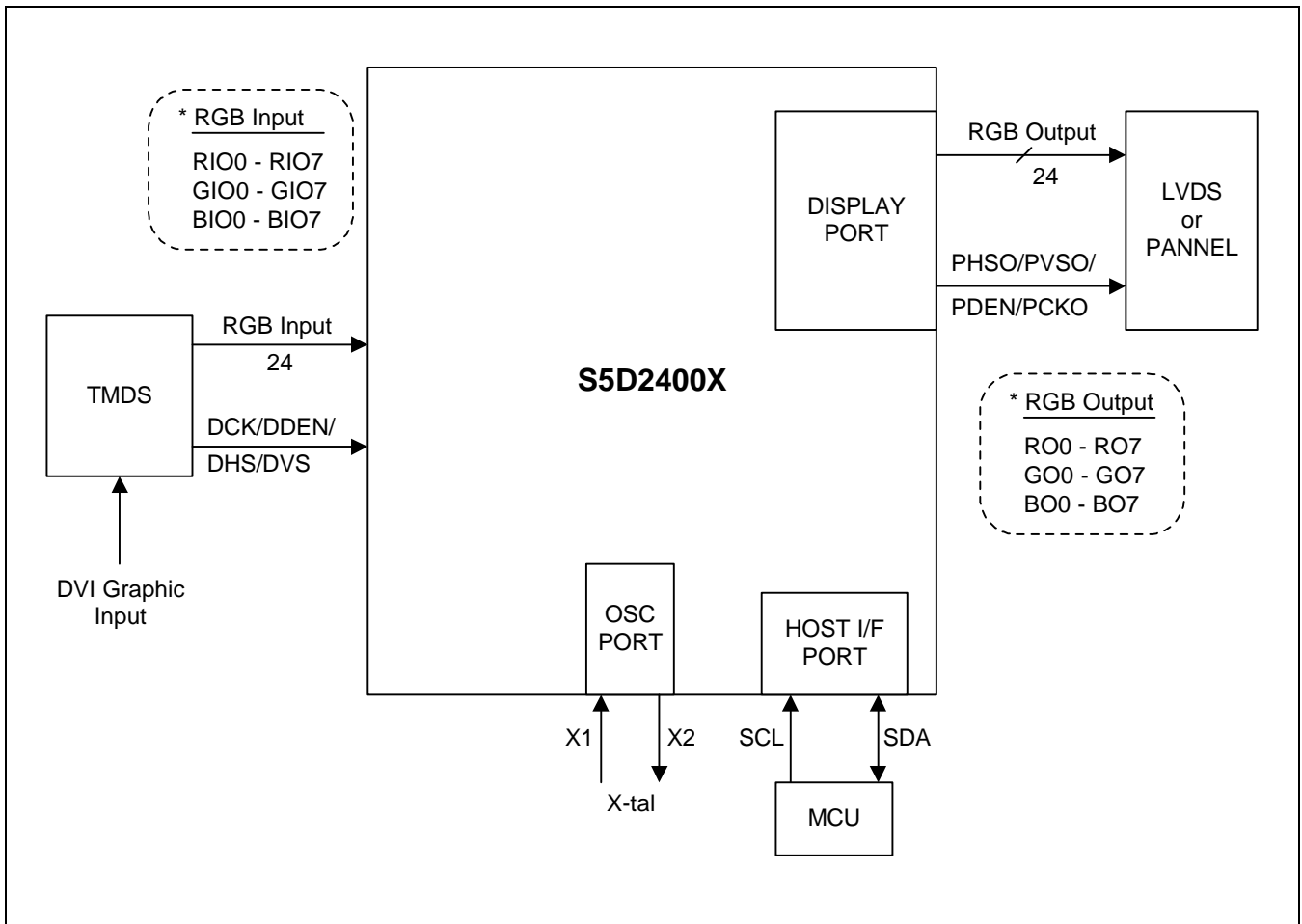


Figure 5. S5D2400X System Block Diagram (DVI Input to Single RGB Output)

3.2 FUNCTIONAL BLOCK DIAGRAM

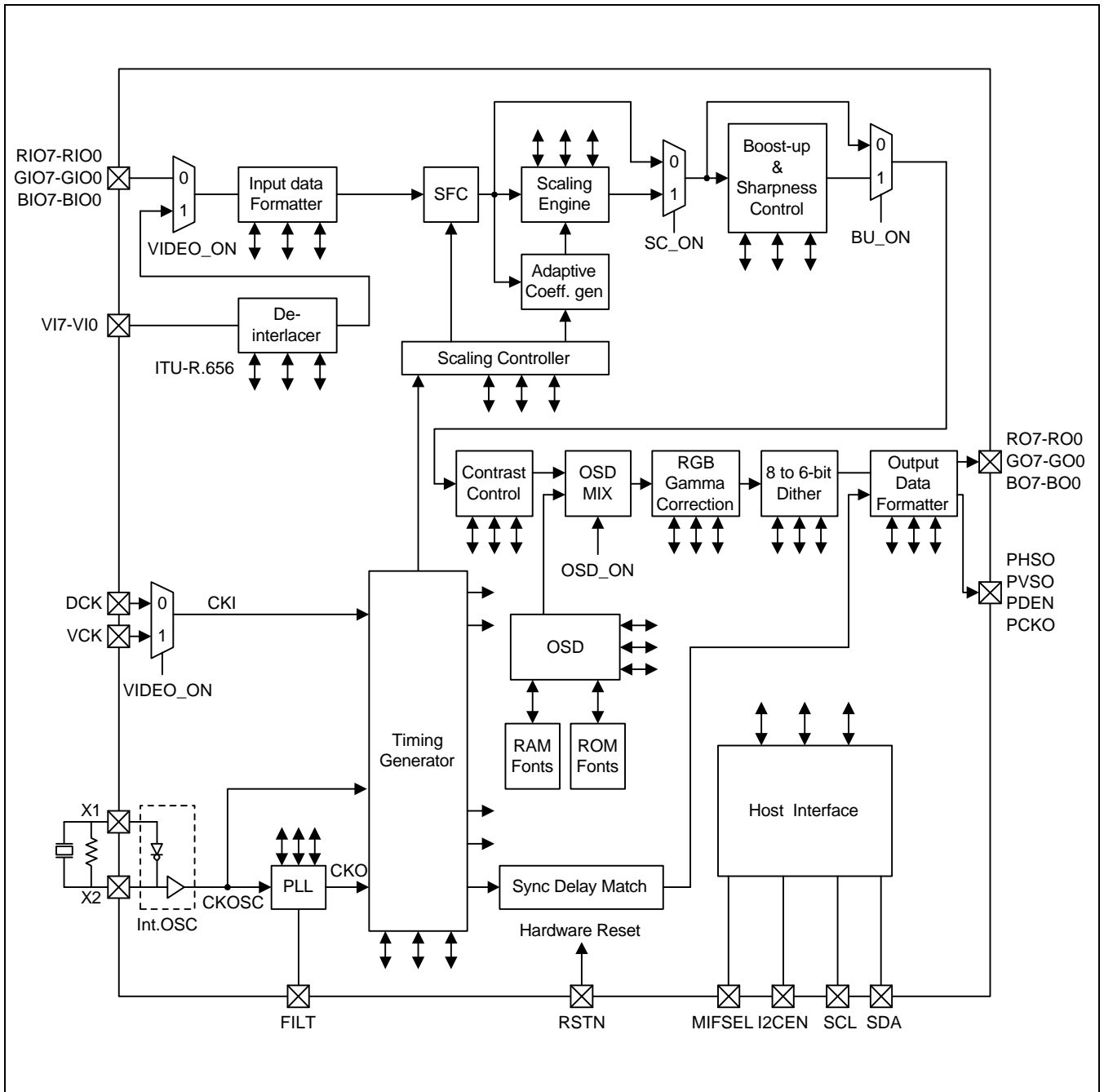


Figure 6. S5D2400X Functional Block Diagram

4 SOLUTION CIRCUIT FOR APPLICATION

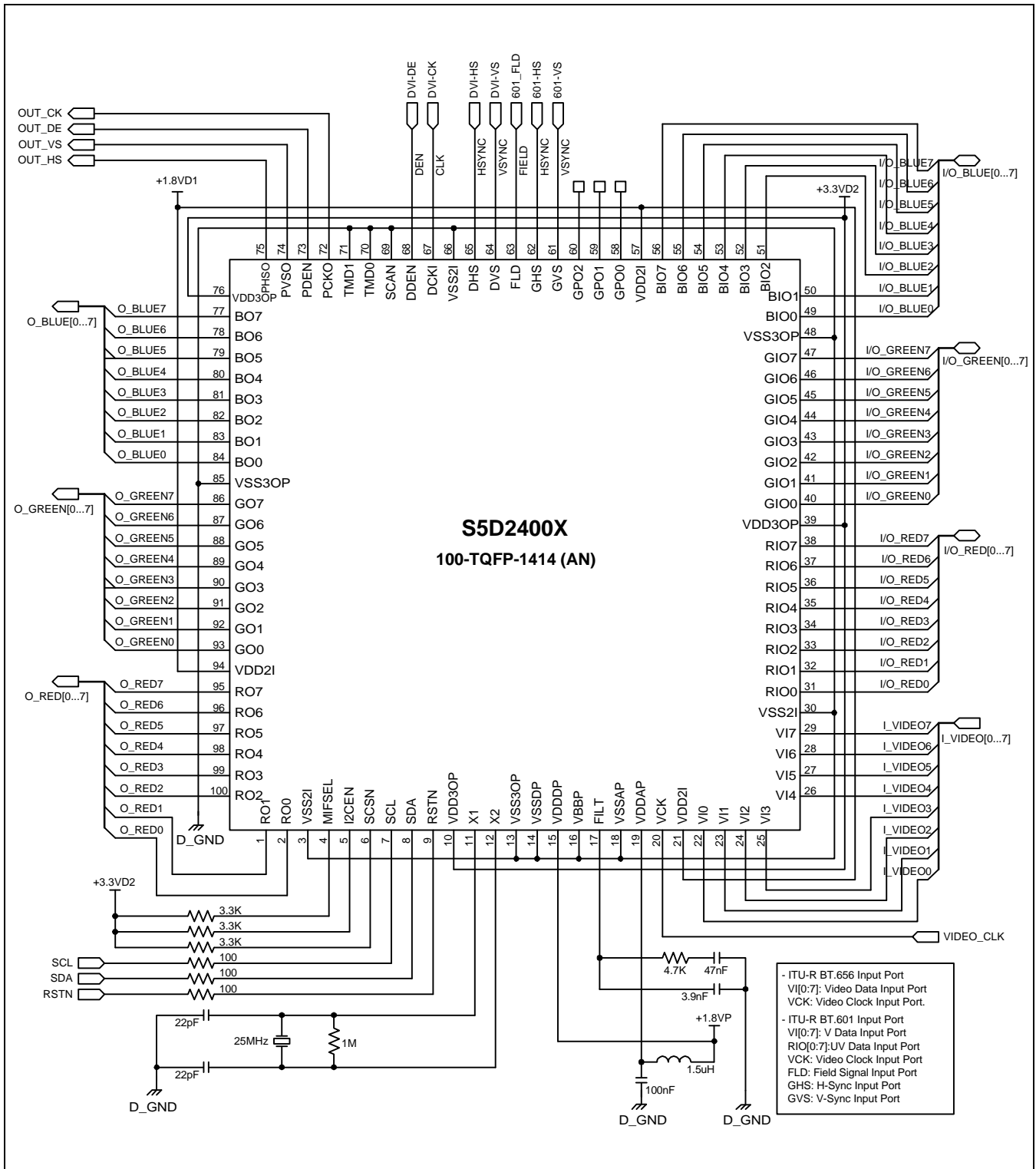


Figure 7. S5D2400X Solution Circuit for Application

5. FUNCTIONAL DESCRIPTION

5.1 CLOCK SYSTEMS AND SYSTEM OPERATION MODES

5.1.1 Clock Systems

The chip supports switching of Separate-RGB signal or ITU-R BT.656/601 protocol video signal data. The Separate-RGB data input clock is DCK, and the ITU-R BT.656/601 format video signal input clock is VCK. The external X-tal oscillation clock X1 is a Free-Run Clock (Recommended 25MHz) which is used as the source clock of PLL in creating data fetch and output clock for host interface. The external clock is created by internal PLL based on the X1 frequency input in accordance with the scaling factor, and is sent to the scaling output terminal and the Panel Display Clock (PCKO). In other words, the clock system selects DCK/VCK as the external clock, uses the free-run clock X1 as the source of output clock and for host I/F, and creates the output clock based on the scaling factor in the internal PLL.

In order to reduce power consumption, it is possible to control the clock system to selectively enable/disable Scaler, OSD, De-Interlacer, Boost-Up and other blocks. In the DPMS Mode, input and output clock is disabled, and only the free-run X1 clock is enabled.

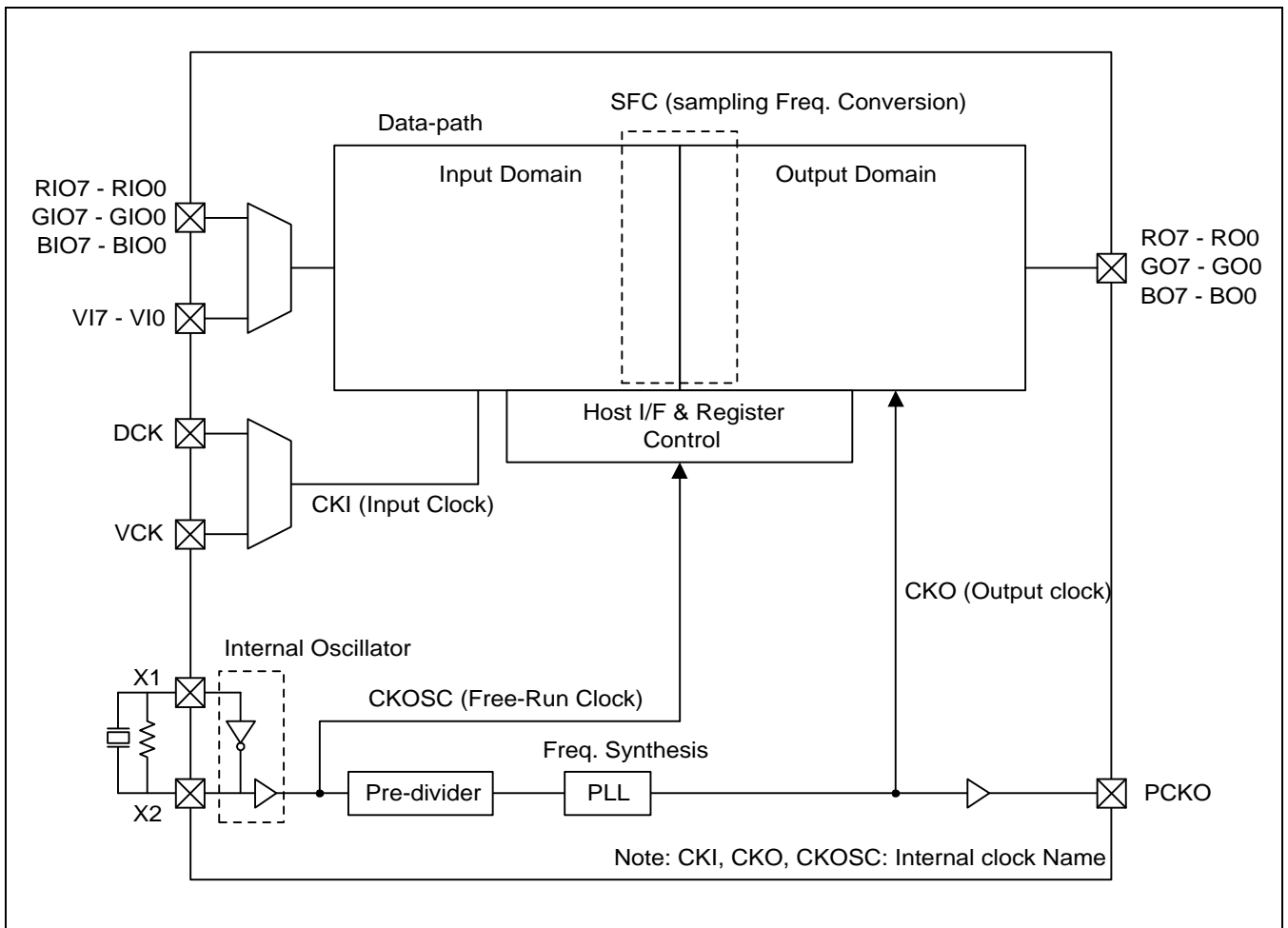


Figure 8. Internal Clock System Diagram

5.1.2 System Operation Modes

The operation mode is divided, depending on the application system, into separate RGB signal input so that the signal can be used in the flat panel display, and processing of video signal entered to ITU-R BT.656/601. The built-in auto tuning function and the de-interlace function may operate against each other. In this way, power consumption can be minimized through management of the functional block.

The table below shows the example of On/Off operation sets. In the DPMS mode, all the functional blocks are off, and only the host interface function works by X-tal clock X1. In the separate RGB input mode, only the BASIC_ON register must be ON for simple 1:1 action. It is possible to expand, in the system level, the operation mode set which is not described in the table.

Mode	ITU-R BT.656 VIDEO_ON	Common				Remark
		SC_ON	BU_ON	OSD_ON	BASIC_ON	
DPMS (No Sync)	X	X	X	X	X	Standby (X1 Clock)
Bypass 1	X	X	X	X	O	Sep. RGB (No Scale)
Bypass 2	X	X	X	O	O	Sep. RGB No Scale + OSD
Bypass 3	X	X	O	X	O	Sep. RGB No Scale + BU
Scale Up/Down 1	X	O	O	O	O	Sep. RGB All Operation
Scale Up/Down 2	O	O	X	O	O	ITU-R BT.656 Scale + OSD
Scale Up/Down 3	O	O	O	X	O	ITU-R BT.656 Scale + BU
Scale Up/Down 4	O	O	O	O	O	ITU-R BT.656 All Operation

NOTES:

1. Ref. Register Map (0x0001[6:0])
2. "O" → ON (Logical "H"), "X" → OFF (Logical "L")
3. Description
 - ◆ VIDEO_ON : De-Interlace ON / OFF for ITU-R BT.656/601 Video Mode (separate-RGB or ITU-R BT.656/601 Mode Selection)
 - ◆ SC_ON : Scaler ON / OFF
 - ◆ BU_ON : Boost-Up ON / OFF for Image Enhancement
 - ◆ OSD_ON : ON-Screen Display ON / OFF for User Control Mode
 - ◆ BASIC_ON : Basic Logic Path ON / OFF (Always ON except DPMS Mode)

5.2 DE-INTERLACE

The De-Interlace block receives the ITU-R BT.656/601 format data, and converts the luminance data and chrominance data from interlace scan mode to progressive scan mode. The luminance data and chrominance data in progressive scan are converted into Red/Green/Blue (RGB) data. The ITU-R BT.656 format data are separated into horizontal sync, vertical sync, field information, luminance data and chrominance data, and ITU-R BT.601 format data are separated into luminance data and chrominance data with horizontal sync, vertical sync and field information received through the other pin.

5.2.1 Functions

- Horizontal Sync Separation from ITU-R BT.656 Format Data
- Vertical Sync Separation from ITU-R BT.656 Format Data
- Field Information Separation from ITU-R BT.656 Format Data
- Luminance Data Separation from ITU-R BT.656 Format Data
- Chrominance Data Separation from ITU-R BT.656 Format Data
- Interlace to Progressive Scan Conversion for Luminance and Chrominance Data
- Red / Green / Blue (RGB) Data Conversion from Luminance / Cb / Cr (YCbCr) Data

5.2.2 ITU-R BT.656 Format Data Separation

The ITU-R BT.656 format data separation block separates horizontal sync, vertical sync, field information, luminance data and chrominance data from the ITU-R BT.656 format data input.

Horizontal sync is in low state in blanking interval, and in high state in active interval. Vertical sync is in low state in blanking interval and in high state in active interval. F is in high state in odd field, and in low state in even field. The active data are a set of Cb/Y/Cr/Y.

5.2.3 Interlace to Progressive Scan Conversion

The Interlace to Progressive Scan Conversion (IPC) block converts the field structure of interlace scan into the frame structure of progressive scan. In other words, 60 Hz / 30 frame (60 field) interlace scan is changed into 60 Hz / 60 frame progressive scan. In interlace to progressive scan conversion, the progressive scan line of 1 frame becomes double of the interlace scan line. In S5D2400X, you can select whether to double the line or maintain the line as it is when converting scan.

5.2.4 YCbCr to RGB Conversion

The YCbCr to RGB conversion block converts the Y / Cb / Cr data into the Red / Green / Blue data.

5.3 TIMING GENERATOR

The timing generator makes timing for S5D2400X, and delivers the value required to make PCKO (output clock). Using the input HS and VS, the block generates PHSO, PVSO and PDEN for output sync, and the signals made with the optimum timing for each block are sent to other blocks. TG also delivers the value required for PCKO. It sends the MCU setting value to internal PLL.

5.3.1 Output Timing Generation

Using input HS and VS, TG generates the output sync (PHSO, PVSO and PDEN). The active data area must be set in input HS and VS. As shown in the following figure, set HIA_STR (0x0012, 0x0013), HIA_END (0x0014, 0x0015), VIA_STR (0x0016, 0x0017), VIA_END (0x0018, 0x0019), HIAS (0x0020, 0x0021) and VIAS (0x0022, 0x0023).

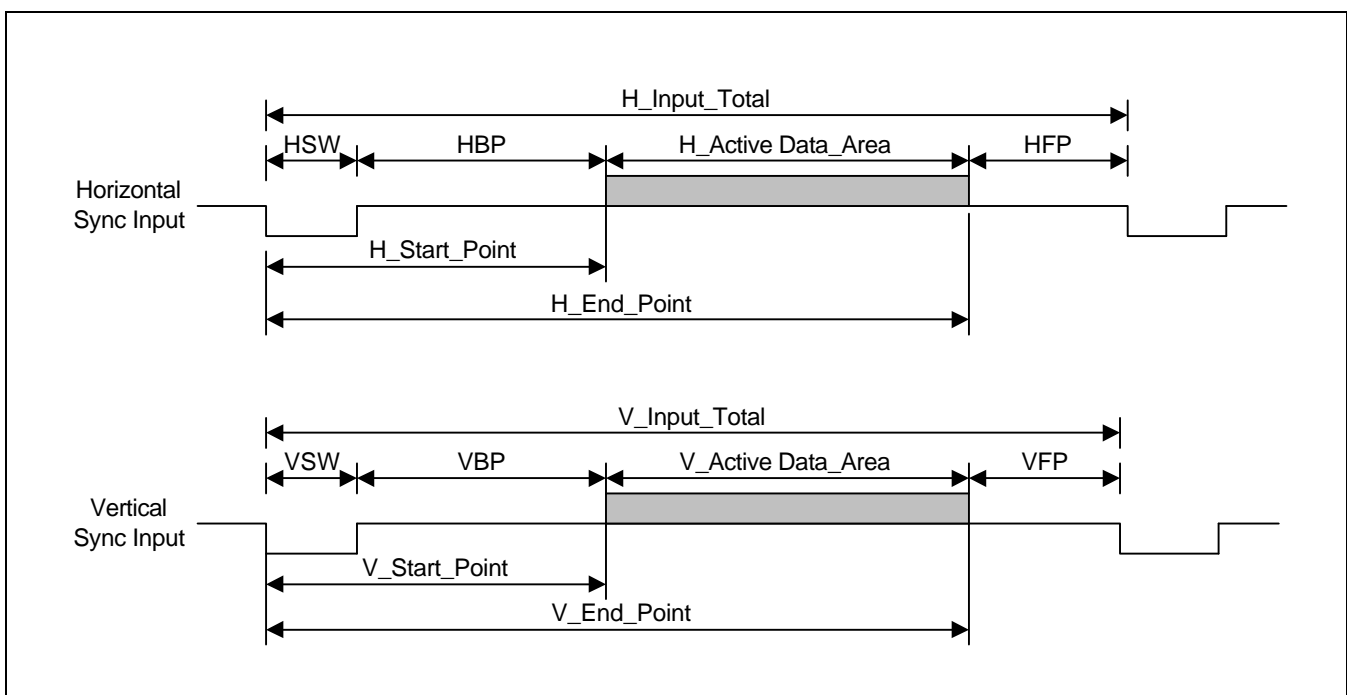


Figure 9 Output Timing Generation

The output signal can be set in HOF (0x001A), HOSW (0x001B), HOBP (0x001C, 0x001D), VOFP (0x001E), VOSW (0x001F), HOAS (0x0024, 0x0025), VOAS (0x0026, 0x0027).

5.4 SCALER

The scaler of S5D2400X operates in the following three modes (Scale-Up, Scale-Down, Bypass).

5.4.1 Scale-Up

The scaler can perform scale-up from VGA to XGA (VGA → SVGA, VGA → XGA, SVGA → XGA) in the DVI mode, and from VGA to 100MHz (VGA → SVGA, VGA → XGA, VGA → 100 MHz, SVGA → XGA, SVGA → 100 MHz, XGA → 100 MHz) in the ITU-R BT.656/601 mode. Different scaling ratio may be applied to H/V (Horizontal/Vertical) direction.

5.4.2 Scale-Down

The scaler can perform scale-down from XGA to VGA (XGA → SVGA, XGA → VGA, SVGA → VGA), and different scaling ratio may be applied to H/V directions.

5.4.3 Bypass

In the bypass mode, the ratio between input and output image is 1:1. In this case, power consumption is decreased if the scaler is OFF (0x001[1]). The bypass mode can be used together with the scale-up mode. In order to use the two modes together, set Bypass (1:1) to horizontal direction and Scale-Up (VGA → XGA) to the vertical direction.

5.5 BOOST-UP

The boost-up block provides you a clear screen.

5.5.1 Adaptive Contrast Control

This function provides a clearer view of a part of or the entire screen by sorting the color to find the maximum, minimum and average value and perform the contrast control processing, and replacing the color with the adaptively calculated color.

5.5.2 Adaptive Brightness Control

This function provides a brighter screen based on a given LUT value. LUT is 0 ~ 255, and is mapping by 1:1.

5.5.3 Image Sharpness Control

The image sharpness control processing provides a more distinctive view of each color by increasing sharpness of boundary of each color.

5.5.4 Color Compensation

A color can be distorted on the screen and may look like a completely different color. The color compensation circuit corrects this problem and maintains the original color.

5.5.5 Boost Up Sub Zone

Boost Up function recognizes the current status of the screen, and reflects the result on the screen. The screen area to be recognized is called "sub zone". Setting the sub zone is necessary because the screen may be affected by other data than the actual video image.

5.6 OSD (ON-SCREEN DISPLAY)

OSD function provides outward GUI between TFT_LCD Monitor and End-User, enabling the user to easily control the environment of TFT-LCD monitor.

OSD supports up to 512 ROM fonts; 16 MCF (Multi-Colored Font) and 464 SF (Standard Font). OSD can be set on certain area of the screen with certain size.

5.6.1 OSD Fonts

1) ROM Font

- 7 languages
- 464 Standard Fonts (SF)
- 16 Multi-Colored Font (MCF)

2) RAM Font

- User Definable Font
- Max. 28 SF, Max. 9 MCF

3) Font RAM Structure

Font RAM is assigned of 1008 addresses (from 0x3FFF to 0x43EE). Where, 1008 is $(8 \text{ row} * 28 \text{ fonts}) * 2 = 504 * 2$. $1008/28 = 36$, and therefore, 36 addresses are assigned to a font. Because the host interface transports data in the unit of 8 bits, in order to configure a font of $12*18$ as shown in Figure 10, the upper 4 bits and the lower 8 bits of 1line (12 bits) are assigned as an address. The upper 4 bits are transported as the even address and the lower 8 bits are transported as the odd address to Font RAM, respectively.

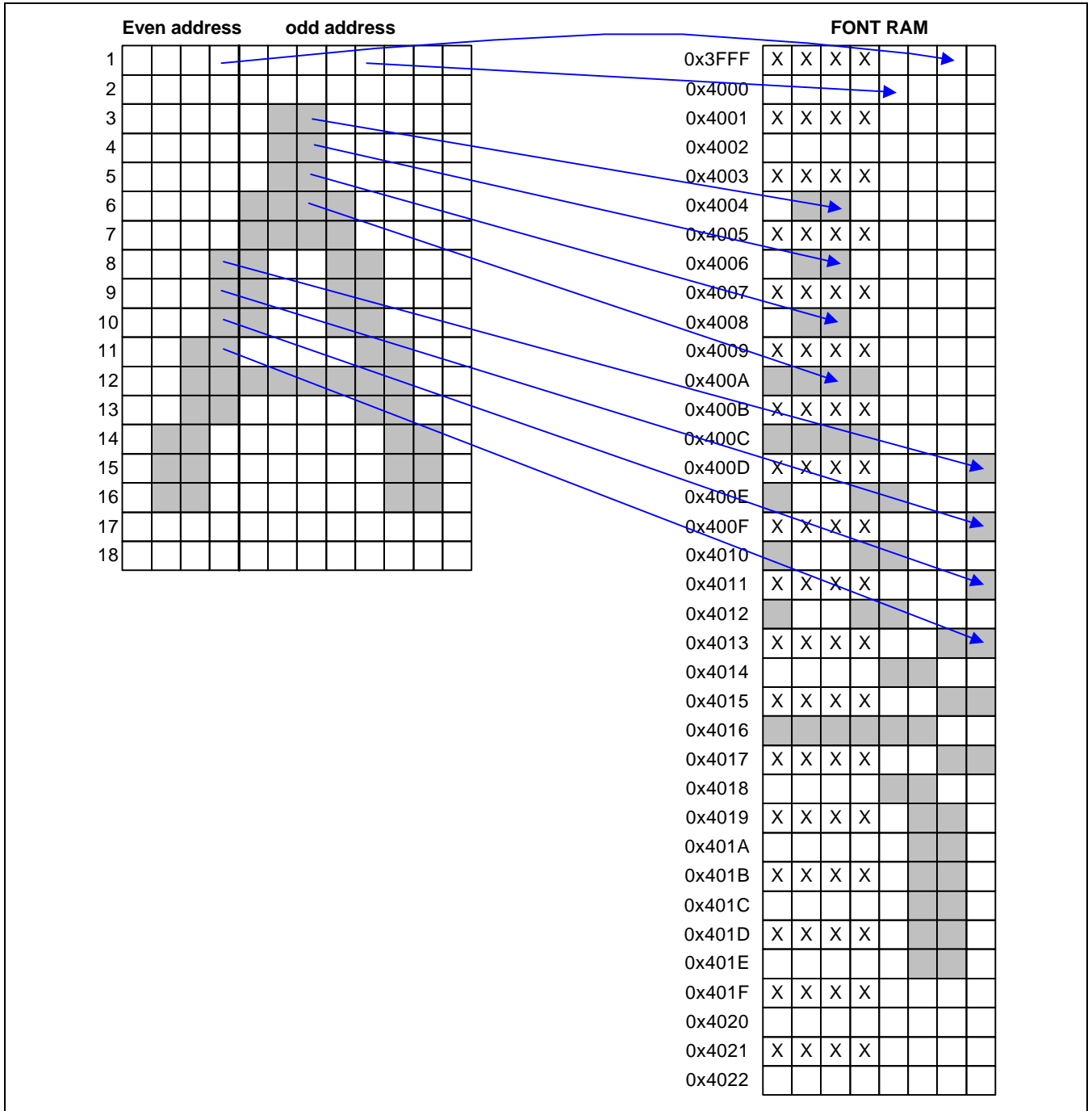


Figure 10. OSD Font RAM

4) Display RAM Structure

Display RAM is assigned of 900 addresses (0x2000 ~ 0x2383). As $900/450 = 2$, 2 addresses are assigned to a display Ram cell. Because the host interface transports data in the unit of 8 bits, in order to form the display RAM cell that uses 16 bits as a cell, 2 addresses must be transported. Figure 11 shows the structure of display RAM cell.

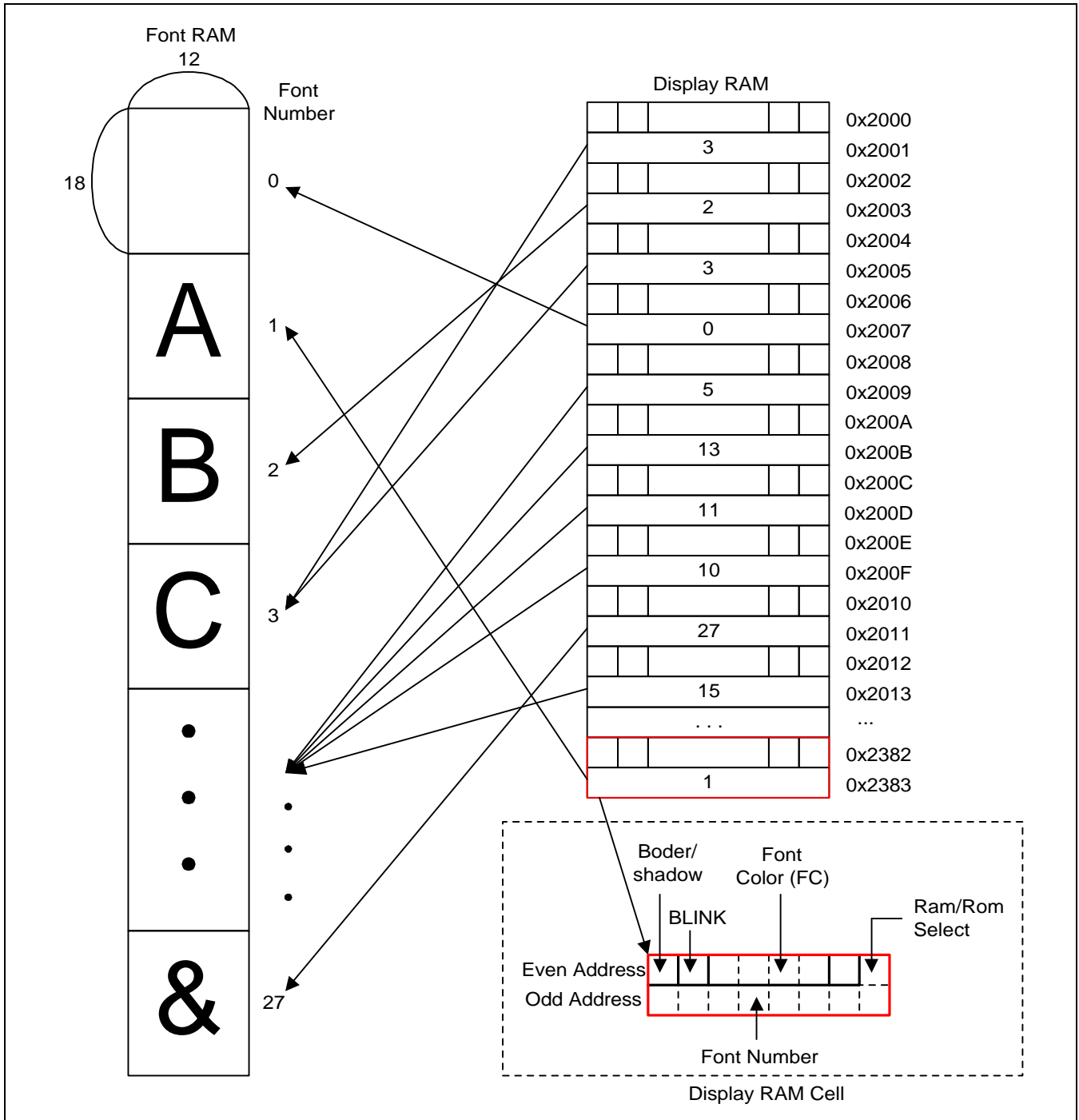


Figure 11. OSD Display RAM

5) Font RAM Clear

This function clears the font RAM based on rising edge detect. The font RAM is cleared by power on reset or FTRAM_CLRN Register. The operation time is 1 Clock, and no delay is made.

The refresh region indicates that "0" value will be given to the entire memory.

Down load or clear works only when OSD_ON Register is On.

In basic operation the font RAM clear function is not required. Using the function in basic mode may cause data loss or other critical problems.

6) Display RAM Clear

This function clears display RAM based on the rising edge detect. The RAM is cleared by power on reset or DSRAM_CLRN Register.

The operation time is 1 Clock, and no delay is made.

5.6.2 OSD Windows

1. Flexible OSD Size:
 - Displays up to 64 fonts in horizontal within the range of 450 fonts
 - Displays up to 64 fonts in vertical within the range of 450 fonts
2. Up to 4 multiple Windows (1 Main Window + 4 Multiple Windows)
3. Up to 32 Windows color including intensity
4. Programmable multiple Windows shadow color/size
5. Fine Windows bordering
6. Pop up / down-able multiple Windows
7. Font position mapping based multiple Windows horizontal/vertical start / end point adjustment
8. Transparency: Input image / OSD image mix.

5.6.3 System Description

OSD stores ROM and font RAM address and features on the display RAM, displays the font and its features at the designated position, and displays on the screen the features designated in OSD register.

1) FONT

OSD font consists of 12 × 18 (width × length) pixels, and is divided into character and raster when displayed on the screen.

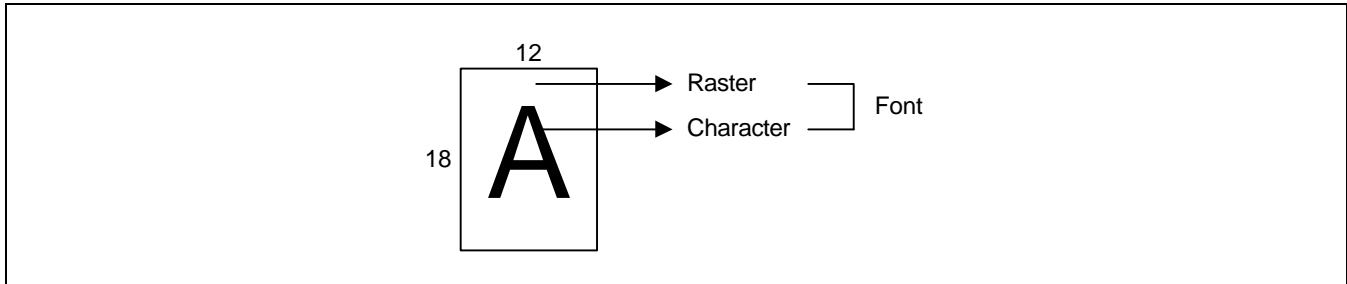


Figure 12. OSD FONT Structure

Font color can be controlled by FC of display RAM. Each font can have 16 character colors and 16 raster colors. FC value is used as a reference of LUT to control character color and raster color.

2) User Definable OSD area

OSD area is defined with the number of OSD horizontal fonts and the number of OSD vertical fonts to be displayed on the screen by OSD_HFONT[5:0] and OSD_VFONT[5:0]. OSD_HFONT and OSD_VFONT are assigned of 6 bits each, generating 64 horizontal/vertical fonts respectively. Because the maximum size of display RAM is limited to 450, it must meet OSD_HFONT*OSD_VFONT ≤ 450. (RAM Address 0 ~ 449) If OSD_HFONT is set to 30 and OSD_VFONT to 10, OSD area is displayed as shown below. In this case, Addresses 0~299 of the display RAM are used for display.

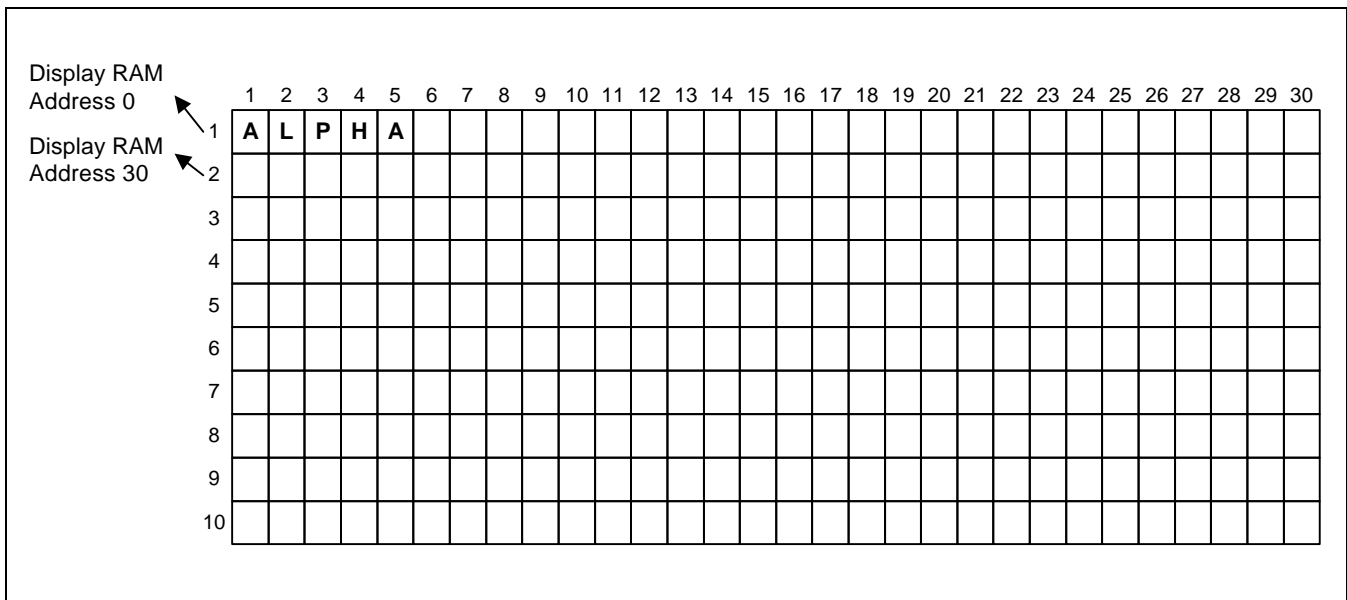


Figure 13. OSD Display RAM Structure

5.6.4. Functions

1) OSD Position

Start position of OSD can be changed via OSD_HSP and OSD_VSP of the OSD register.

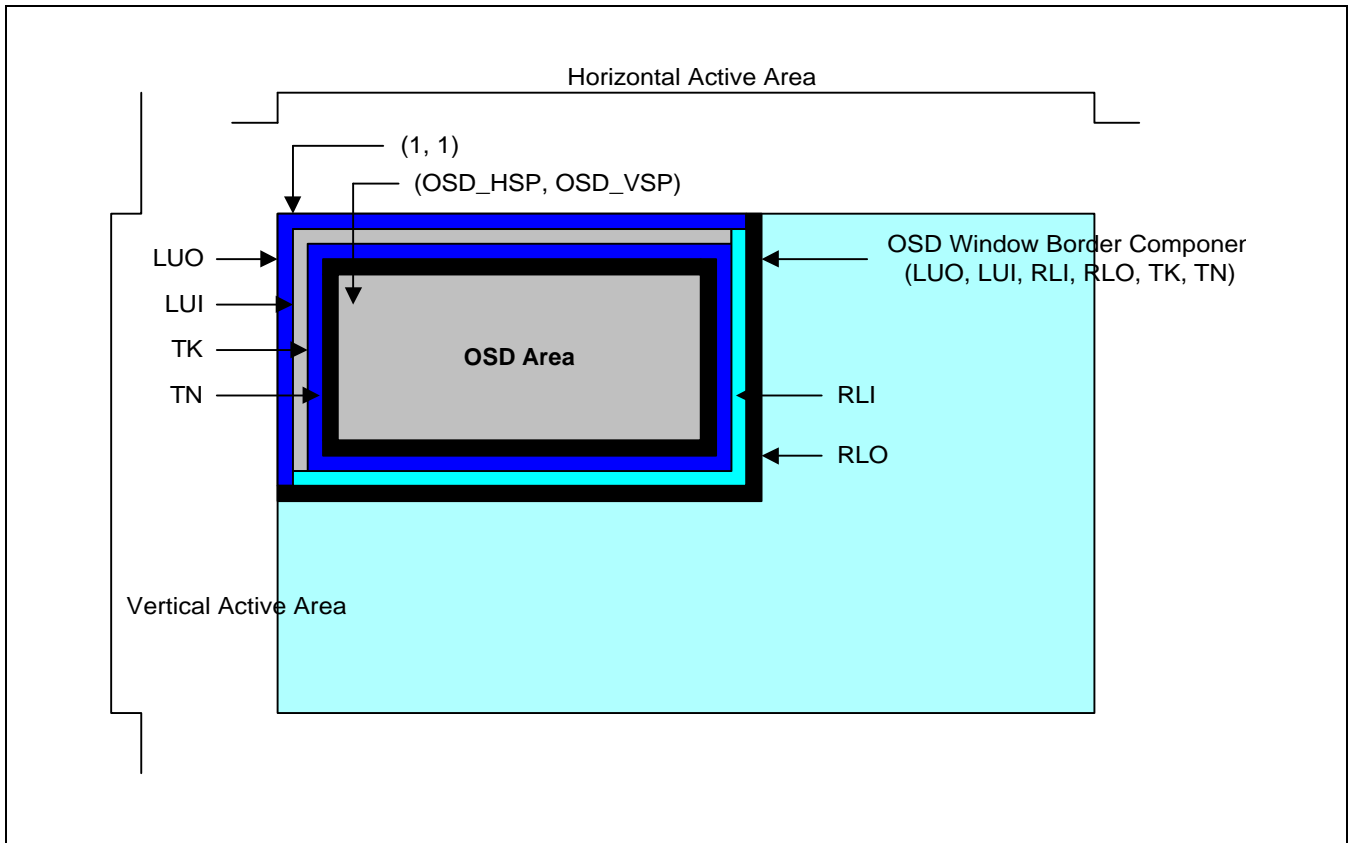


Figure 14. OSD Position

2) Font size control

OSD fonts are saved in FontRAM or ROM in the unit of 12 bits, displayed as a 12*18 font through No. 18 access and display. The horizontal and vertical size of a font can be 1x, 2x, 3x and 4x through adjustment of CH_HSZ and CH_VSZ.

3) Character Border/Shadow

Character Border/Shadow of a font can be implemented through CH_BDSH_EN setting in OSD register, and with 1 or 0 (1: Border, 0: Shadow) selection of CH_BDSH of display RAM.

4) Blink Control

OSD blink can be controlled by font. Font blinking function is enabled through BL_NTRA (BLink or NoToneRAster) setting and display RAM blink setting.

BLNK_SEL is used to adjust blink duty as the blink function is enabled.

BLNK_SEL	Blink OFF	Blink ON
0	0.5 sec	0.5 sec
1	1 sec	0.5 sec
2	0.5 sec	1 sec
3	1 sec	1 sec
4	1.5 sec	1.5 sec
5	2 sec	1 sec
6	1 sec	2 sec
7	2 sec	2 sec

BLNK_C supports the color inversion of the blinking character. If BLNK_C is enabled, the complementary color of the font raster color is displayed in the character area during blink-off. If BLNK_C is reset, the raster color is displayed in the character area during blink-off.

5) Intensity control

OSD intensity can be controlled by frame. It is possible to control 16 colors by character / raster in reference to LUT of Display RAM FC (Font Color), or 32 colors by frame by toggling INTENSITY bit.

6) Multi-Colored font control

OSD provides 512 ROM fonts to display the icon, generating Multi-language OSD icon. Out of 512 ROM fonts, 464 fonts are the standard fonts (Single-Color) and 16 ($16 \times 3 = 48$) fonts are multi-colored fonts. Each multi-colored font consists of three color attribute ROM fonts. The three fonts make a multi-colored font with OR operation. In order to access a multi-colored font, the R-color attribute font is addressed. For example, 1D0h, 1E0h and 1F0h address indicate R, G and B-color attribute fonts respectively. By addressing 1D0h, a multi-colored font can be accessed through OR operation of 1D0h, 1E0h and 1F0h color attribute fonts.

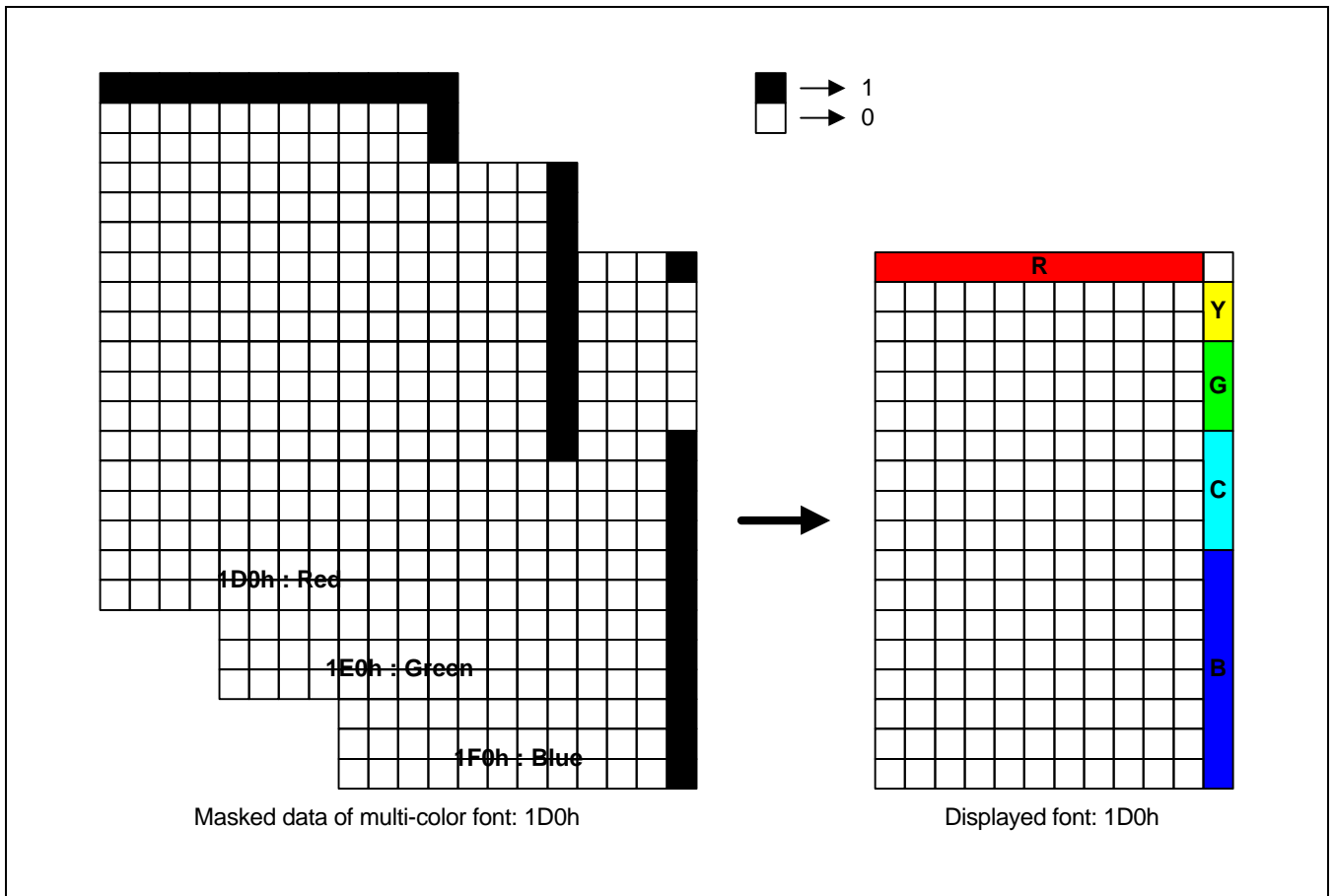


Figure 15. OSD Multi Color Font Structure

The multi-colored font (MCF) of the RAM font is made in the same way as the Standard Font (SF) is formed. MCF count can be adjusted through the N_MCF value, and 28 fonts except MCF are used as SF.

7) External OSD control

If the external OSD is enabled (EXT_OSD_SEL == 1), the external OSD expresses the color in reference to LUT of S5D2400X_OSD. For color mapping, refer to 4-3. Receiving R, G, B, I, EN input from the external OSD, S5D2400X_OSD decodes the 4 inputs except EN, and displays each color value. External OSD input is delayed by 2Pixel clock before displayed. Even if external OSD is used, S5D2400X_OSD supports half tone. In order to apply half tone to font raster and not to apply half tone to the character, the values between 0000b and 1011b shall be assigned to R, G, B, I.

(OSD_TONE == 0, CH_TONE == 0)

8) Blank font control

By accessing and displaying 000h address of ROM, it is possible to display only input image within the OSD area. This ROM 000h address called a blank font has several useful functions. For example, multiple Windows can be displayed on the OSD area only. The function can be used to display multiple Windows without the OSD area.

9) Row Space

A row space indicates the space in vertical direction between the fonts displayed on OSD. S5D2400X_OSD assigns 0-15 to ROW_SP to implement the row space.

A row space is displayed on the screen via interworking with Character Vertical Size (CH_VSZ).

In other words, if CH_VSZ is 1 and ROW_SP is 3, the row space actually displayed is 6 pixels. The maximum number of vertical pixels of a row space to be displayed is 4*15 (CH_VSZ == 3, when ROW_SP == 15).

If row space is enabled, the raster is extended as many as the row space pixels on the top or bottom of a font.

Figure 18 shows the details. (when ROW_SP == 1, and CH_VSZ == 0).

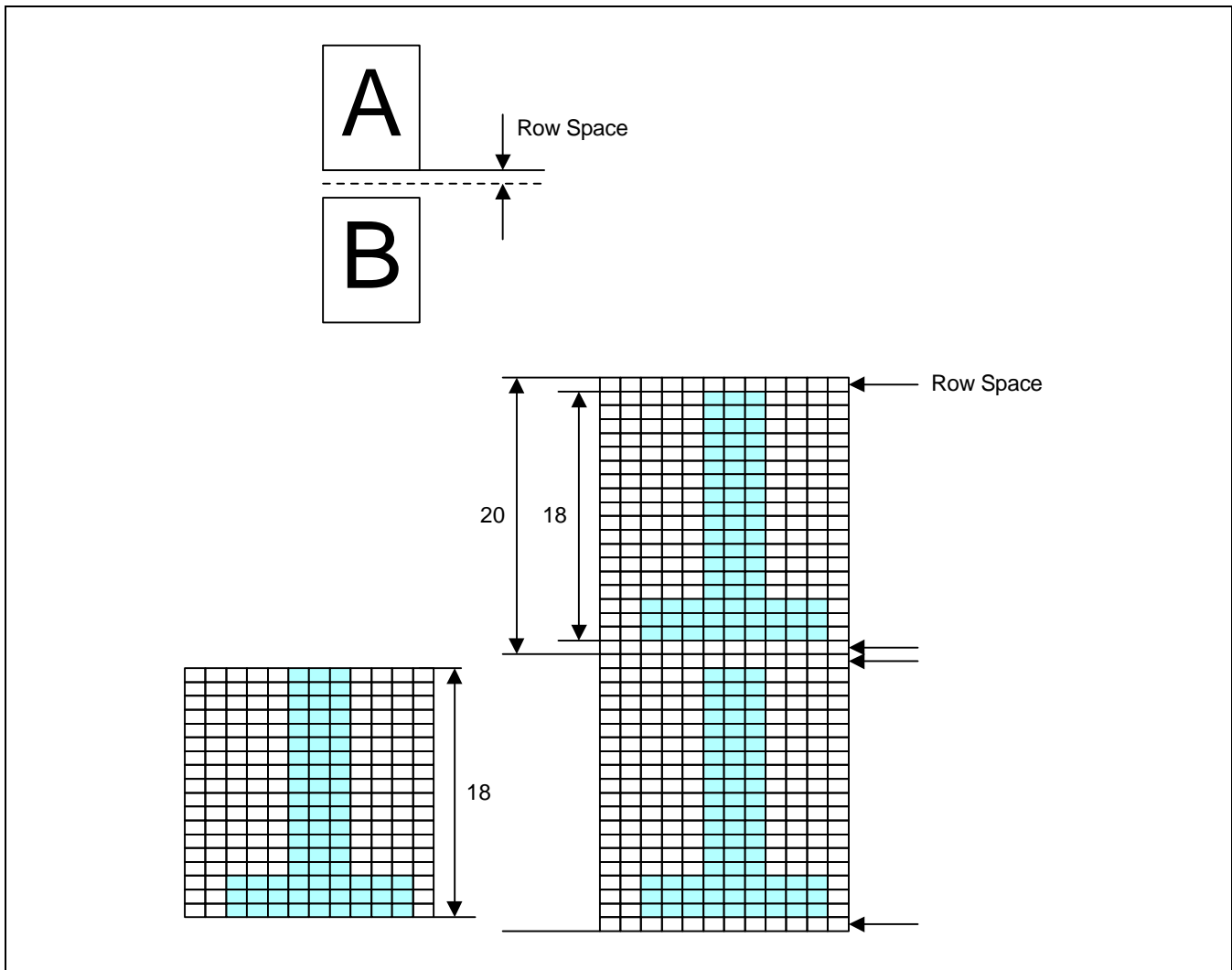


Figure 16. OSD Row Space

10) Half Tone (Transparency) Control

Half tone of S5D2400X_OSD is made via mixing of input image and OSD image. Where, OSD_TONE[1:0] is used as a weight for mixing of image and OSD image.

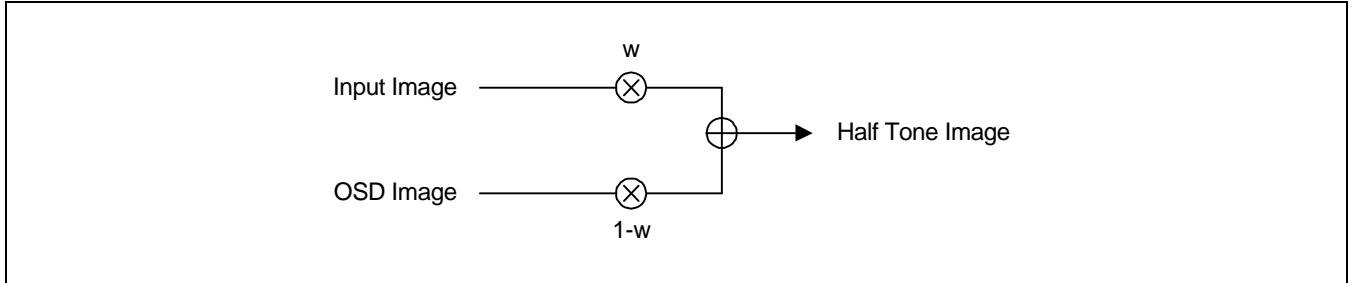


Figure 17. Half Tone Block

5.7 GAMMA

The gamma correction block performs gamma compensation to complement the TFT-LCD panel features. The block divides the input signal level to various sections, makes non-linear feature curve for each section, and by linear interpolation of each section, performs gamma compensation. In other words, the block divides the input into sections, and changes the output value of each section to deform specific curves for gamma compensation. An input signal has 8 bits digital level, it is evenly divided into 32 sections with the space of 8.

The block receives output value for each evenly spaced level from MCU, performs non-linear gamma compensation, and performs linear interpolation for the values between the levels. Gamma compensation is applied to each of RGB data in the same way, but the output values can be changed respectively.

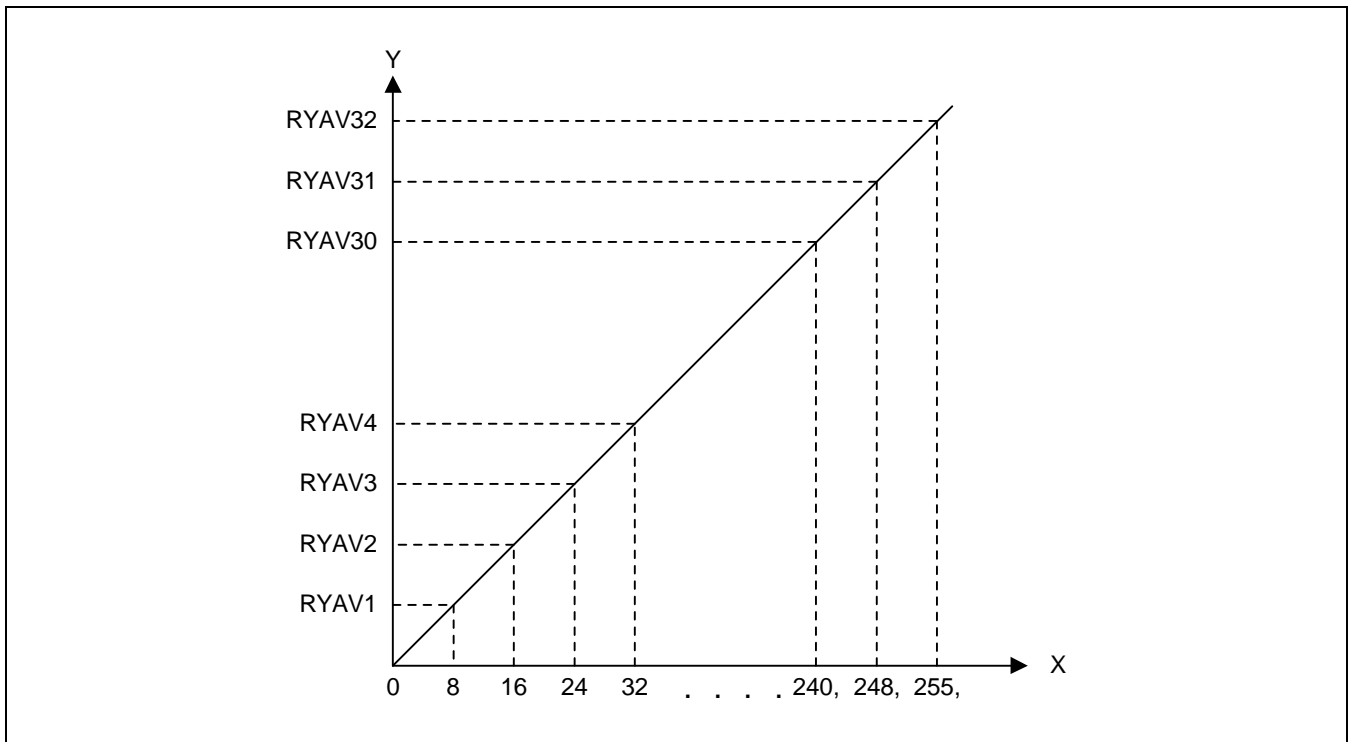


Figure 18. R-Channel Gamma Correction

5.8 CONTRAST CONTROL

Contrast block is applied to all pixels, and can control the boost-up area and other areas respectively. Blacklevel and brightness play the role of offset, and contrast works as gain. Each pixel value is acquired in the following process.

$$R_{out} = [R_{in} - \text{Blacklevel}(\text{Red})] * \text{Contrast}(\text{Red}) + \text{Brightness}(\text{Red})$$

$$G_{out} = [G_{in} - \text{Blacklevel}(\text{Green})] * \text{Contrast}(\text{Green}) + \text{Brightness}(\text{Green})$$

$$B_{out} = [B_{in} - \text{Blacklevel}(\text{Blue})] * \text{Contrast}(\text{Blue}) + \text{Brightness}(\text{Blue})$$

5.9 DITHER

5.9.1 Enable Dither

The dithering block supports the following 4 modes.

Table 8. Dither Mode

DTH_MODE[1:0]	Operation mode (I/O and RGB data valid bit count)
000	Bypass mode (8-bit RGB input, 8-bit RGB output)
101	ED mode (8-bit RGB input, 6-bit RGB output)

5.9.2 Error Diffusion (ED) Method

The following figure illustrates the block diagram of error diffusion dithering. The block diagram is made for R, but can be applied to G and B in the same manner.

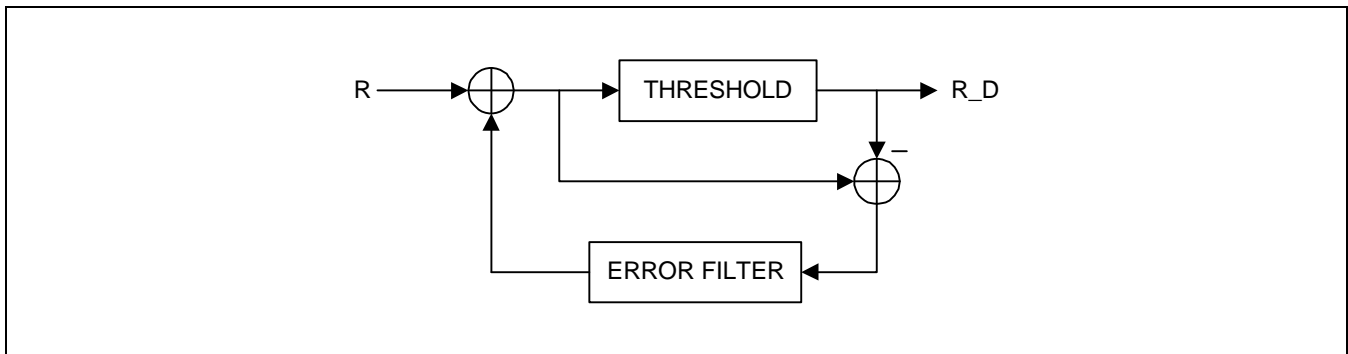


Figure 19. Error Diffusion Architecture

The threshold block cuts off the lower 2 bits. Therefore the cut 2 bits are used as the input to the error filter.

5.10 TEST PATTERN GENERATOR (TPG)

TPG internally generates a pattern for sync and test without input sync and data. In order to enable TPG, TEST_PAT_ON (0x0001[7]) must be High.

5.10.1 TPG Sync Signals

Figure 20 illustrates the internally generated sync.

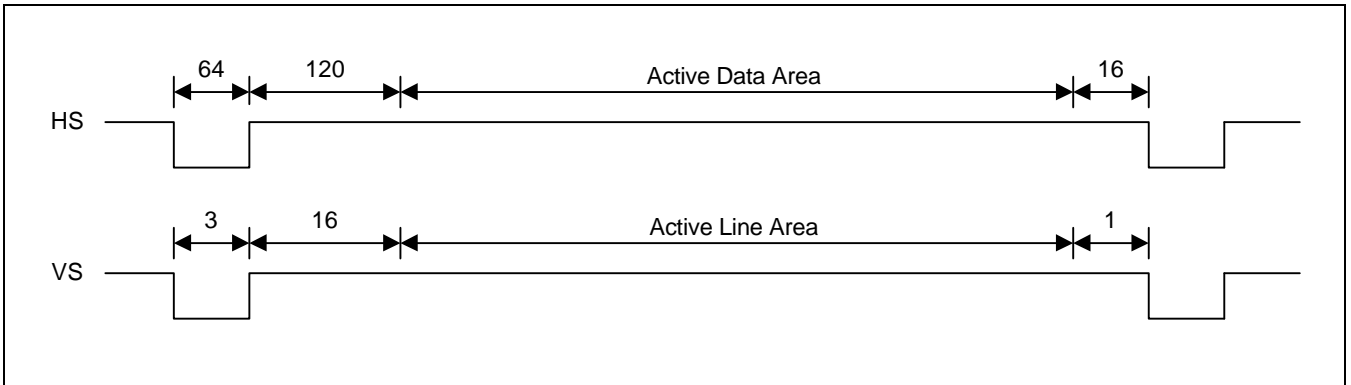


Figure 20. TPG Sync Signals

The active data area and the active line area in Figure 20 are determined by TP_RESOLUTION (0x0006 [7:6]).

Table 9. Active Pattern Areas

PATTERN_SIZE	0	1	2
ACTIVE AREA (H*V)	VGA (640*480)	SVGA (800*600)	XGA (1024*768)

5.10.2 Test Patterns

The pattern to be used as input data to scaler is selected by TP_TYPE(0x0006[5:0]). For Bit [5], 0 is pass and 1 inverts image. For Bit [4], 0 sends normal pattern and 1 sends H/V ramp waveform. Other bits are described in Figure 21.(a) and (b). Figure 21.(a) illustrates the ramp waveform selection in H/V direction when Bit [4] is 1. Figure 22 (a) shows the example. Figure 21.(b) shows the example when bit [4] is 0. If the lower 4bits are 0~5, the screen pattern is as displayed in Figure 22.(b). The other values from 6~15 display the white screen.

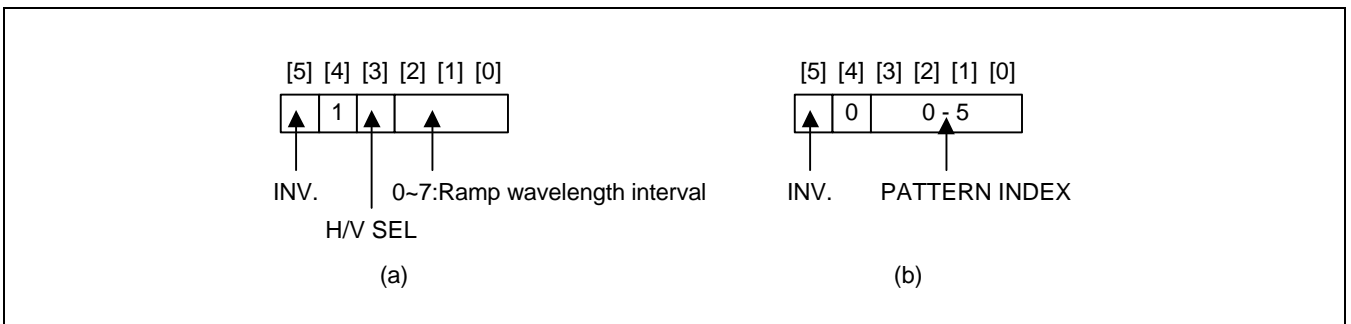


Figure 21. Test Pattern Generation Method

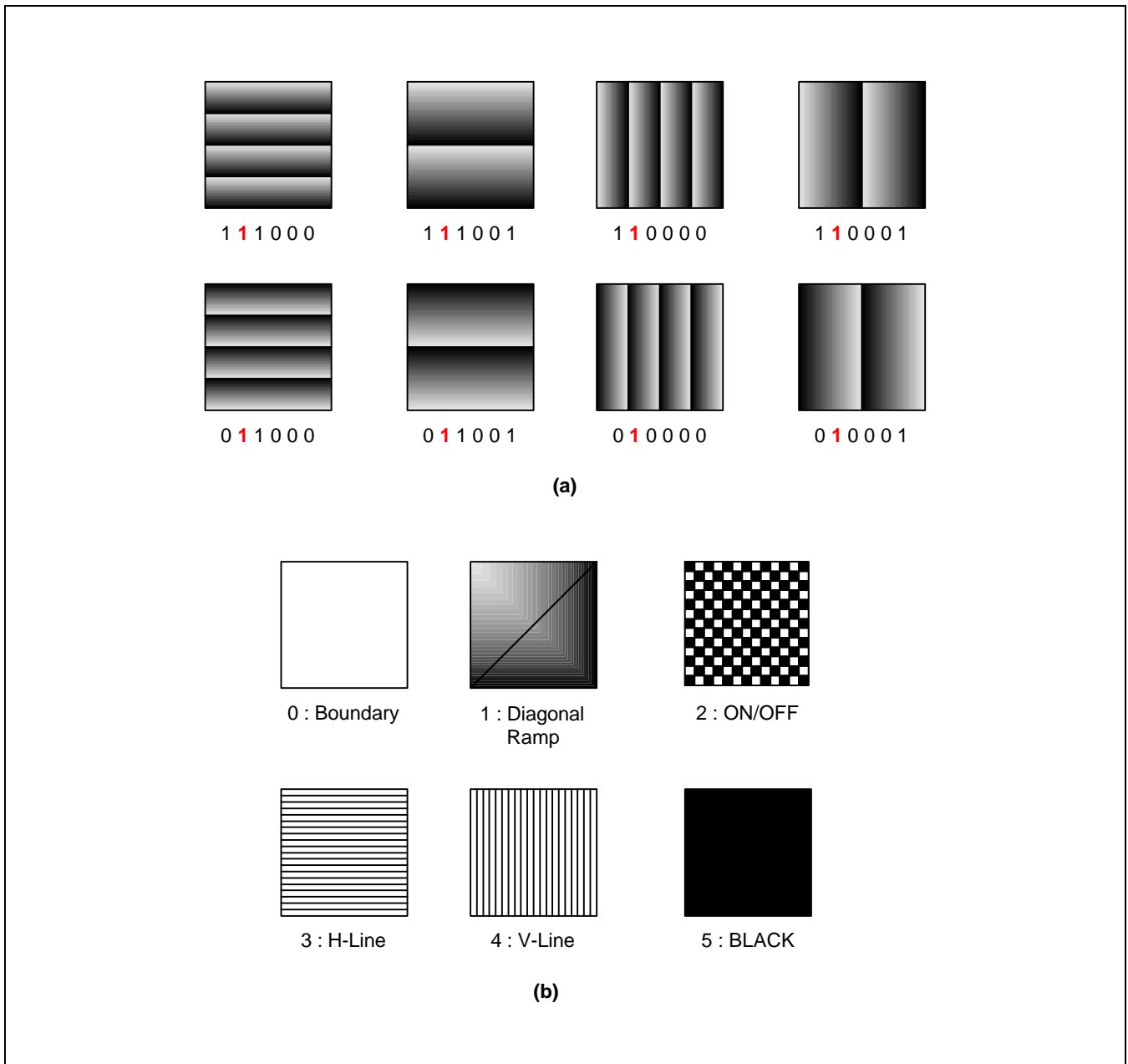


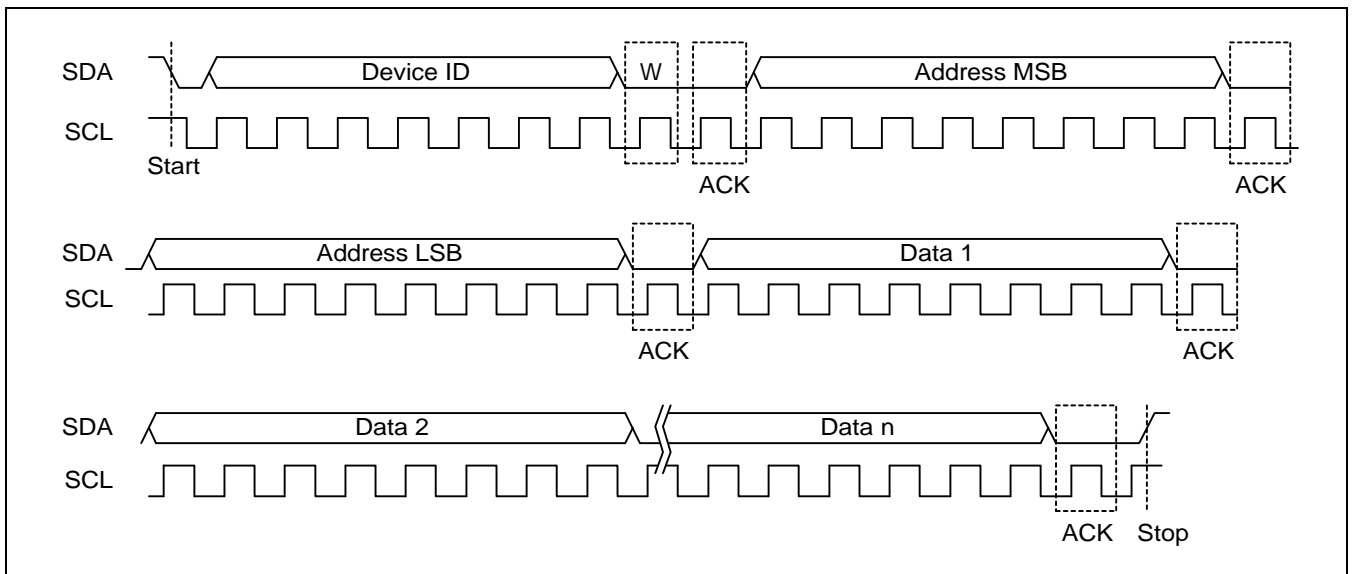
Figure 22. Built-in Test Patterns

5.11 I2C HOST INTERFACE PROTOCOL

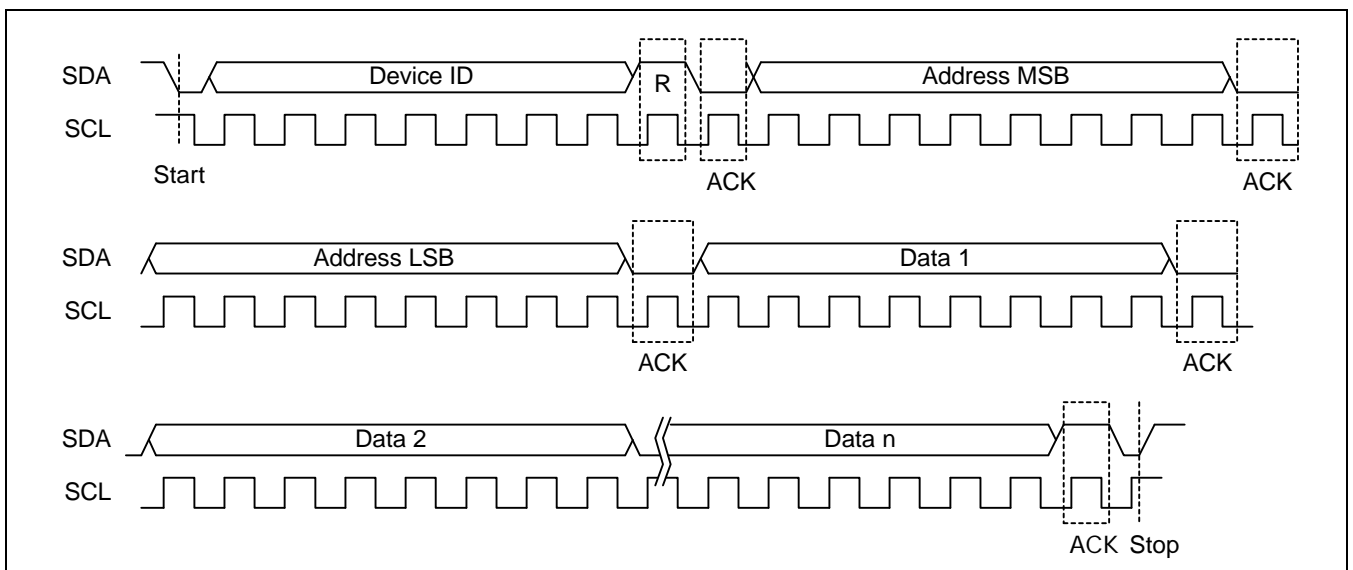
S5D2400X supports data communication through I2C protocol based host interface. The slave address for a device ID is 7 bits (binary "0000101"). The address is made with 15 bits with 8 bits data depth. Therefore, in order to access an address, 2 bytes (Address MSB, Address LSB) are indexed with 1 byte data depth. Because the address bits are 15 bits, the 1 byte of the address MSB is Binary "X A₁₄ A₁₃ A₁₂ A₁₁ A₁₀ A₉ A₈", and the 1 byte of the address LSB is Binary "A₇ A₆ A₅ A₄ A₃ A₂ A₁ A₀".

5.11.1 Timing Chart (Data sequence for register write/read of n registers)

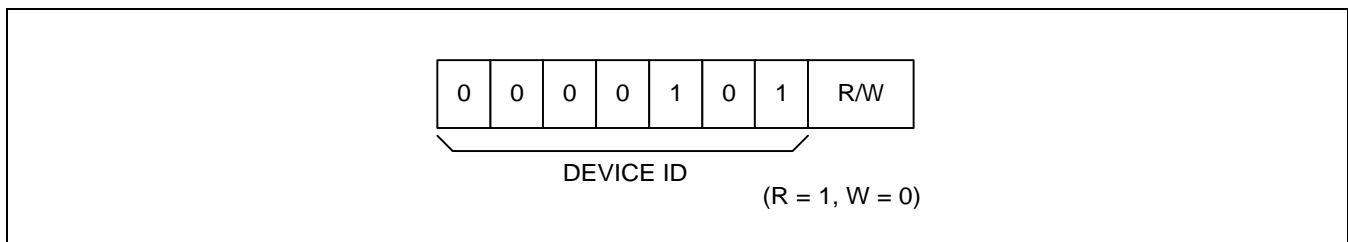
Write Data Sequence



Read Data Sequence



The figure below shows the device ID and read/write byte for the slave address in the above timing chart.



Because an address is 15 bits, the 1 bit of the address MSB is remained. Set 0 or 1 (Don't Care : X) for the 1 bit.

5.11.2 Example

Write to one register

- Send Start Signal
- Send Device ID Byte (R/W Bit = LOW)
- Send Address MSB
- Send Address LSB
- Send Data to Address
- Send Stop Signal

Write to four consecutive register

- Send Start Signal
- Send Device ID Byte (R/W Bit = LOW)
- Send Address MSB
- Send Address LSB
- Send Data 1 to Address
- Send Data 2 to (Address + 1)
- Send Data 3 to (Address + 2)
- Send Data 4 to (Address + 3)
- Send Stop Signal

Read from one register

- Send Start Signal
- Send Device ID Byte (R/W Bit = HIGH)
- Send Address MSB
- Send Address LSB
- Receive Data from Address
- Send Stop Signal

Read form four consecutive control registers

- Send Start Signal
- Send Device ID Byte (R/W Bit = HIGH)
- Send Address MSB
- Send Address LSB
- Receive Data 1 from Address
- Receive Data 2 from (Address + 1)
- Receive Data 3 from (Address + 2)
- Receive Data 4 from (Address + 3)
- Send Stop Signal

6 REGISTER MAP

6.1 GLOBAL CONTROL REGISTERS

Bits	Register Name	Function
0x0000		GLOBAL_RESET (Default: 0 x 01) R/W
7:2		Reserved
1	FREE_RUN	Pseudo sync RUN mode (1: ON, 0: OFF (Default)) - When to use : Power on, mode switch, and recovery from Over Sync/Under Sync DPMS
0	SOFT_RSTN	Resets the chip in software level except User Register (The register defined in the spec data sheet). (Low Active) - When to use: Power ON and mode switch - How to use: Set the chip to 0, reset, and then to 1. (Reset time must be 1uS or higher (1 Clock) without delay.) The last "N" of the Register Name indicates Active Low Soft Reset.

0x0001		GLOBAL_BLOCK_CONTROL (Default: 0 x 03) R/W
7	TEST_PAT_ON	Blocks input regardless of external data input status, and displays the internal test pattern. Test Pattern (1: ON, 0: OFF (Default))
6	VIDEO_ON	VIDEO Mode & DVI Mode (1: VIDEO Mode, 0: DVI Mode (Default))
5		Reserved
4	BU_ON	Boost Up (1: ON, 0: OFF (Default)). Do not use in the DVI mode.
3	OSD_ON	OSD (1: ON, 0: OFF (Default))
2		Reserved
1	SC_ON	- Up to 10x for Scaling-Up and up to 1/2x for Scaling-Down - The screen size is not changed when switching OFF SC_ON when the target resolution and the input resolution are the same (1x Scaling). - In bypass status, only scaling is bypassed. Therefore, PMS setting must be performed. (1: Scaler ON, 0: Scaler OFF (Default))
0	BASIC_ON	In the Normal operation status, Basic logic must be always On. (1: Basic Logic ON (Default), 0: Basic Logic OFF)

0x0002		GLOBAL_IO_CONTROL (Default: 0 x 00)	R/W
7:4		Reserved	
3	PWM1_ON	Pulse Width Modulation1 1: ON (PWM_DATA1(0x000D 7:0h) signal is sent through GP01 Pin) 0: OFF(GPO1(0x000B 1h) signal is sent through GP01 Pin)	
2	PWM0_ON	Pulse Width Modulation0 1: ON (PWM_DATA0 (0x000C 7:0h) signal is sent through GPO0 Pin) 0: OFF(GPO0(0x000B 0h) signal is sent through GPO0 Pin)	
1		Reserved	
0	PLL_PWR_SAVE	Scaler PLL Power Down Mode for system CLK generation (CKO) (1: PLL Power Down Mode, 0: Normal Mode)	

0x0003		GLOBAL_OUTPUT_CONTROL (Default: 0 x 38)	R/W
7:6		Reserved	
5	ROUT_EN	RO (R-channel Output) Enable of PIN NO 1~2, 95~100 ROUT (1: Enable (Default), 0: Disable)	
4	GOUT_EN	GO (G-channel Output) Enable of PIN NO 86~93 GOUT (1: Enable (Default), 0: Disable)	
3	BOUT_EN	BO (B-channel Output) Enable of PIN NO 77~84 BOUT (1: Enable (Default), 0: Disable)	
2	RIN/OUT_EN	Determines whether to use RIO of PIN NO 31~38 as output or input. If the OCHMD bit is 0, RIO is used as input regardless of RIN/OUT_EN bit control. If the OCHMO bit is 1, RIO is used as input or output depending on RIN/OUT_EN bit control. (1: Output, 0: Input (Default))	
1	GIN/OUT_EN	Determines whether to use GIO of PIN NO 40~47 as output or input If the OCHMD bit is 0, GIO is used as input regardless of GIN/OUT_EN bit control. If the OCHMO bit is 1, GIO is used as input or output depending on GIN/OUT_EN bit control. (1: Output, 0: Input (Default))	
0	BIN/OUT_EN	Determines whether to use BIO of PIN NO 49~56 as output or input. If the OCHMD bit is 0, BIO is used as input regardless of BIN/OUT_EN bit control. If the OCHMO bit is 1, BIO is used as input or output depending on BIN/OUT_EN bit control. (1: Output, 0: Input (Default))	

0x0004		GLOBAL_PHASE_CONTROL ((Default: 0 x 00)	R/W
7:6		Reserved	
5	CKI2_PHASE	Changeable 2-Times Input Clock Phase (1: Phase Inverse, 0: Normal)	
4:0		Reserved	

0x0005		GLOBAL_CKO_CONTROL (Default: 0 x 00)	R/W
7:6		Reserved	
5:4	CKO_SEL	CKO Clock source Select (Always 00) (00: PLL Output is used 01,10,11: Not used)	
3	CKO2_PHASE	Changeable 2-Times Scaler Output Clock Phase (1: Phase Reverse, 0: Normal)	
2:0	PCKO_PHASE	Scaler Output Clock(PCKO) Time Delay - PCKO_PHASE[2] : PCKO Phase Inverse. - PCKO_PHASE[1:0] : X ns Delay (X = PCKO_PHASE[1:0])	

0x0006		GLOBAL_PATTERN_CONTROL (Default: 0 x 80)	R/W
7:6	PATTERN_SIZE	Pattern Size select (00: VGA, 01: SVGA, 10: XGA (Default), 11: Unused)	
5:0	PATTERN_SEL	Selecting Test Pattern Type (Default: 0)	

0x0007		GLOBAL_POSITION_CONTROL (Default: 0 x 00)	R/W
7:0		Must be 08h	

0x000A		GLOBAL_IO_MODE_DEFINE (Default: 0 x 00)	R/W
7:5	DITHER_MODE	Selecting Dither mode type to change from 8 bits to 6 bits on the Scaler out. 000 : Bypass 101 : Error Diffusion Other values should not be used.	
4:3		Reserved	
2	ICHMD	Scaler Input Channel Mode (0: Single Input (Always Low))	
1	OCHMD	Scaler Output Channel Mode Select (1: Dual Output, 0: Single Output)	
0	OCHSEL	Select A or B channel from Scaler Output Dual Channel. - This bit is enabled when ADDR (0x000A[1]) is Dual. 0: In the Dual mode, data are sent from Channel A. 1: In the Dual mode, data are sent from Channel B.	

0x000B		GLOBAL_GPO_DATA (Default: 0 x 00)	R/W
7:6	PWM_PRE_SCALE	When pulse width modulation is used, this bit determines, based on the oscillation clock, the level of PWM duty level to be divided. (00: Oscillation, 01: 2_Divided, 10: 4_Divided, 11: 8_Divided)	
5	PWM_EN	Pulse Width Modulation Enable (1: Enable, 0: Disable)	
4:3		Reserved	
2	GPO2	General Purpose Output 2	
1	GPO1	General Purpose Output 1	
0	GPO0	General Purpose Output 0	

0x000C		GLOBAL_PWM_DATA1 (Default: 0 x 00)	R/W
7:0	PWM_DATA0	Pulse Width Modulation 0. Controls duty in the High section.	

0x000D		GLOBAL_PWM_DATA2 (Default: 0 x 00)	R/W
7:0	PWM_DATA1	Pulse Width Modulation1. Controls duty in the High section.	

6.2 TIMING GENERATOR CONTROL REGISTERS

Bits	Register Name	Function	
0x0010		TG_MODE_SEL (Default: 0 x 18)	R/W
7	HVSO_DET_ON	Must be always 1. If the bit is "0", HVSO_DET is not controlled.	
6	HVSO_DET	- In Invert, the bit initializes TG Sync, and detects again to create output sync. Event Driven PHSO and PVS0 Detect (Low to High, High to Low) by Write Value Change Operation	
5		Reserved	
4:3	DET_FRAME	TG Detection Start Frame (1 ~ 4 Frame): (Default: 3) : The number of frames required to detect sync after the HVSO_DET value is changed.	
2	PREDIV_CKSEL	Pre-Divider clock Select (1: CKI, 0: CKOSC (X1, Default))	
1:0	PLL_FIN_SEL	PLL FIN Signal Select (0: PRE_CK → XGA (Default), 1: Not used, 2, 3: HS → when scaling rate is small) If HS is used in MCU Control, select PRE_CK to stabilize CLK, and then, select HS.	

0x0012		TG_HIA_STR_h (Default: 0 x 01)	R/W
7:3		Reserved	
2:0	HIA_STR[10:8]	Manual Horizontal Input Active Start Point (Horizontal Input sync Width + Back Porch)	

0x0013		TG_HIA_STR_l (Default: 0 x 10)	R/W
7:0	HIA_STR[7:0]	Manual Horizontal Input Active Start Point	

0x0014		TG_HIA_END_h (Default: 0 x 05)	R/W
7:3		Reserved	
2:0	HIA_END[10:8]	Manual Horizontal Input Active End Point (Horizontal Input sync Width + Back Porch + Active Size)	

0x0015		TG_HIA_END_I (Default: 0 x 0F)	R/W
7:0	HIA_END[7:0]	Manual Horizontal Input Active End Point	
0x0016		TG_VIA_STR_h (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	VIA_STR[10:8]	Manual Vertical Input Active Start Point (Vertical Input sync Width + Back Porch)	
0x0017		TG_VIA_STR_I (Default: 0 x 1F)	R/W
7:0	VIA_STR[7:0]	Manual Vertical Input Active Start Point	
0x0018		TG_VIA_END_h (Default: 0 x 03)	R/W
7:3		Reserved	
2:0	VIA_END[10:8]	Manual Vertical Input Active End Point (Vertical Input sync Width + Back Porch + Active Size)	
0x0019		TG_VIA_END_I (Default: 0 x 1E)	R/W
7:0	VIA_END[7:0]	Manual Vertical Input Active End Point - H/V_Start/end Point is changed when VIA_END[7:0] is controlled.	
0x001A		TG_HOFP (Default: 0 x 10)	R/W
7:0	HOFP	Horizontal Output Front Porch	
0x001B		TG_HOSW (Default: 0 x 60)	R/W
7:0	HOSW	Horizontal Output Sync Width	
0x001C		TG_HOBP_h (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	HOBP[10:8]	Horizontal Output Back Porch	
0x001D		TG_HOBP_I (Default: 0 x B0)	R/W
7:0	HOBP[7:0]	Horizontal Output Back Porch	

0x001E		TG_VOFP (Default: 0 x 01)	R/W
7		Reserved	
6:0	VOFP	Vertical Output Front Porch	

0x001F		TG_VOSW (Default: 0 x 03)	R/W
7:0	VOSW	Vertical Output Sync Width	

0x0020		TG_HIAS_h (Default: 0 x 04)	R/W
7:3		Reserved	
2:0	HIAS[10:8]	Horizontal Input Active Size	

0x0021		TG_HIAS_I (Default: 0 x 00)	R/W
7:0	HIAS[7:0]	Horizontal Input Active Size	

0x0022		TG_VIAS_h (Default: 0 x 03)	R/W
7:3		Reserved	
2:0	VIAS[10:8]	Vertical Input Active Size	

0x0023		TG_VIAS_I (Default: 0 x 00)	R/W
7:0	VIAS[7:0]	Vertical Input Active Size	

0x0024		TG_HOAS_h (Default: 0 x 04)	R/W
7:3		Reserved	
2:0	HOAS[10:8]	Horizontal Output Active Size	

0x0025		TG_HOAS_I (Default: 0 x 00)	R/W
7:0	HOAS[7:0]	Horizontal Output Active Size	

0x0026		TG_VOAS_h (Default: 0 x 03)	R/W
7:3		Reserved	
2:0	VOAS[10:8]	Vertical Output Active Size	

0x0027		TG_VOAS_I (Default: 0 x 00)	R/W
7:0	VOAS[7:0]	Vertical Output Active Size	
0x0028		TG_PLL_P_h (Default: 0 x 03)	R/W
7:0	PLL_P[15:8]	PLL Programmable Pre-Divider	
0x0029		TG_PLL_P_I (Default: 0 x E8)	R/W
7:0	PLL_P[7:0]	PLL Programmable Pre-Divider	
0x002A		TG_PLL_M_h (Default: 0 x 18)	R/W
7:6		Reserved	
5:0	PLL_M[13:8]	PLL Programmable Main-Divider	
0x002B		TG_PLL_M_I (Default: 0 x 9B)	R/W
7:0	PLL_M[7:0]	PLL Programmable Main-Divider	
0x002C		TG_PLL_S (Default: 0 x 01)	R/W
7:2		Reserved	
1:0	PLL_S	PLL Programmable Post Scaler	
0x002D		TG_PLL_M_FRACT (Default: 0 x 00)	R/W
7:0	PLL_M_FRACT	TG's PLL_M register Fraction bits	
0x0032		TG_A_HACTO_OFFSET_h (Default: 0 x 02)	R/W
7:6		Reserved	
5:0	A_HACTO_OFFSET [13:8]	Automatic Horizontal Output Active Point OFFset Delay - Up Mode: $A_HACTO_OFFSET = HI_{total} * VSTR_OFFSET * Vratio * HTOTratio / 32$ - Down Mode: $A_HACTO_OFFSET = 29 * HTOTratio * Vratio + HI_{total} * VSTR_OFFSET * Vratio * HTOTratio / 32 - 2$	

0x0033		TG_A_HACTO_OFFSET_I (Default: 0 x 90)	R/W
7:0	A_HACTO_OFFSET [7:0]	Automatic Horizontal Output Active Point OFFset Delay	

0x01B0		TG_SYNC_DVI (Default: 0 x 0A)	R/W
7:5		Reserved	
4	D_STOP_SIZE	Size Detection Update Enable (1: Previous Frame Data, 0: Frame Update)	
3	DHS_POL_SEL	TMDS Output DHS Polarity Detection Priority (1: MCU Detection, 0: Internal Detection)	
2	DHS_POL_EXT	TMDS Output DHS Polarity Selection by MCU (DHS_POL_SEL = 1) (1: Positive Type, 0: Negative Type)	
1	DVS_POL_SEL	TMDS Output DVS Polarity Detection Priority (1: MCU Detection, 0: Internal Detection)	
0	DVS_POL_EXT	TMDS Output DVS Polarity Selection by MCU (DVS_POL_SEL = 1) (1: Positive Type, 0: Negative Type)	

0x01B2		TG_DHS_TOTAL_h	RO
7:3		Reserved	
2:0	DHS_HITS[10:8]	DHS Horizontal Input Total Size	

0x01B3		TG_DHS_TOTAL_I	RO
7:0	DHS_HITS[7:0]	DHS Horizontal Input Total Size	

0x01B4		TG_DVS_TOTAL_h	RO
7:3		Reserved	
2:0	DVS_VITS[10:8]	DVS Vertical Input Total Size	

0x01B5		TG_DVS_TOTAL_I	RO
7:0	DVS_VITS[7:0]	DVS Vertical Input Total Size	

0x01B6		TG_DDEN_HIA_STR_h	RO
7:3		Reserved	
2:0	DD_HIA_STR[10:8]	DDEN Horizontal Input Active Start Point	

0x01B7		TG_DDEN_HIA_STR_I	RO
7:0	DD_HIA_STR[7:0]	DDEN Horizontal Input Active Start Point	

0x01B8		TG_DDEN_HIA_END_h	RO
7:3		Reserved	
2:0	DD_HIA_END[10:8]	DDEN Horizontal Input Active End Point	

0x01B9		TG_DDEN_HIA_END_I	RO
7:0	DD_HIA_END[7:0]	DDEN Horizontal Input Active End Point	

0x01BA		TG_DDEN_VIA_STR_h	RO
7:3		Reserved	
2:0	DD_VIA_STR[10:8]	DDEN Vertical Input Active Start Point	

0x01BB		TG_DDEN_VIA_STR_h	RO
7:0	DD_VIA_STR[7:0]	DDEN Vertical Input Active Start Point	

0x01BC		TG_DDEN_VIA_END_h	RO
7:3		Reserved	
2:0	DD_VIA_END[10:8]	DDEN Vertical Input Active End Point	

0x01BD		TG_DDEN_VIA_END_I	RO
7:0	DD_VIA_END[7:0]	DDEN Vertical Input Active End Point	

6.3 DE-INTERLACE CONTROL REGISTERS

Bits	Register Name	Function	R/W
0x0040		(Default: 0 x 38)	R/W
7:6		Reserved	
5	DI_FIELD_POL	FIELD Signal Polarity 1: Odd Field (Field 1) High, Even Field (Field 2) Low - Required Design 0: Even Field (Field 2) High, Odd Field (Field 1) Low - 656 SPEC	
4	DI_HACT_POL	HACT Signal Polarity 1: Active High - Required Design 0: Active Low - 656 SPEC	
3	DI_VACT_POL	VACT Signal Polarity 1: Active High - Required Design 0: Active Low - 656 SPEC	
2	DI_SYNC_GEN	Sync Generation Block Selection 0: Required Design	
1	DI_C_SIGN	Chroma Sign Bit Determination 1: 2's Complementary - Non SPEC 0: Positive Number - SPEC (Required Design)	
0	DI_CBCR_SEL	Cb / Cr Signal Input Type Selection 1: CR Y CB Y CR Y ... - NON_SPEC 0: CB Y CR Y CB Y ... - SPEC (Required Design)	

0x0041		DI_SYNC_POLARITY (Default: 0 x 00)	R/W
7		Reserved	
6	ITU-R BT.656	1: ITU-R BT.601, 0: ITU-R BT.656	
5	DI_HALF_RATE	1: Half_Rate ON, 0: Half_Rate OFF	
4	HALF_YC_POL_INV	Half_Rate Y/C Polarity Inversion	
3	HALF_VS_POL_INV	Half_Rate V-Sync Polarity Inversion	
2	HALF_HS_POL_INV	Half_Rate H-Sync Polarity Inversion	
1	HALF_HACTO_POL_INV	Half_Rate HACTO Polarity Inversion	
0	HALF_FIELD_POL_INV	Half_Rate Field Polarity Inversion	

0x0042		DI_VSO_SEL (Default: 0 x 00)	R/W
7:4	VSO_ODD_SEL	Odd Field V-Sync Select	
3:0	VSO_EVEN_SEL	Even Field V-Sync Select	

0x0043		DI_HOFP (Default: 0 x 0A)	R/W
7:0	DI_HOFP	Horizontal Output Front Porch	

0x0044		DI_HOSW (Default: 0 x 1E)	R/W
7:0	DI_HOSW	Horizontal Output Sync Width	

0x0045		DI_VOFP (Default: 0 x 04)	R/W
7:0	DI_VOFP	Vertical Output Front Porch	

0x0046		DI_VOSW (Default: 0 x 06)	R/W
7:0	DI_VOSW	Vertical Output Sync Width	

0x0047		DI_LINE_START (Default: 0 x 03)	R/W
7:0	DI_LINE_START	Vertical Line Start Point Included Active Vertical Area	

0x0048		DI_LINE_WIDTH_h (Default: 0 x 01)	R/W
7:2		Reserved	
1:0	DI_LINE_WIDTH[9:8]	Vertical Line Width Included Active Vertical Area	

0x0049		DI_LINE_WIDTH_l (Default: 0 x E2)	R/W
7:0	DI_LINE_WIDTH[7:0]	Vertical Line Width Included Active Vertical Area	

0x004A		DI_DEINTERLACE_TYPE (Default: 0x 0F)	R/W
7:4		Reserved	
3:2	DI_DI_YTYPE	Y Interpolation Type (Trade Off of screen blurring and zagging) 0 : Screen blurring < -- > 3 : Noise 0 : Strong Zagging < -- > 3 : Weak Zagging Recommended Value : 1	
1:0	DI_DI_CTYPE	C Interpolation Type (The same value with Y Interpolation Type)	

0x004B		DI_HACTO_MG (Default: 0 x FF)	R/W
7:4	DI_HACTO_ST_MG	HACTO Signal Start Point Margin (-8 ~ +7) : DI_MIN_H = HACTO Start + DI_HACTO_ST_MG	
3:0	DI_HACTO_ED_MG	HACTO Signal End Point Margin (-8 ~ +7) : DI_MAX_H = HACTO End + DI_HACTO_ED_MG	

0x004C		DI_601CLK_PHASE (Default: 0 x 00)	R/W
7:3		Unused	
2:0	DCLK_PHASE	ITU-R BT.601 format Clock Phase	

0x004D		DI_601HV_SEL (Default: 0 x 00)	R/W
7		Unused	
6	EXT_FLD_SEL	1: External Field Select, 0: Internal Field Select	
5	HS601_INV	ITU-R BT.601 H-Sync Inversion	
4	VS601_INV	ITU-R BT.601 V-Sync Inversion	
3:2	V601_ODD	ITU-R BT.601 Odd Field Active Line Select	
1:0	V601_EVEN	ITU-R BT.601 Even Field Active Line Select	

0x004E		DI_601HIA_STR_h (Default: 0 x 00)	R/W
7:1		Unused	
0	DI_601HIA_STR[8]	ITU-R BT.601 Horizontal Input Active Start Point	

0x004F		DI_601HIA_STR_l (Default: 0 x EF)	R/W
7:0	DI_601HIA_STR[7:0]	ITU-R BT.601 Horizontal Input Active Start Point	

0x0050		DI_601VIA_STR (Default: 0 x 11)	R/W
7:0	DI_601VIA_STR	ITU-R BT.601 Vertical Input Active Start Point	

0x0051		DI_601_VIAS_h (Default: 0 x 00)	R/W
7:2		Unused	
1:0	DI_601_VIAS[9:8]	ITU-R BT.601 Vertical Input Active Size	

0x0052		DI_601_VIAS_I (Default: 0 x F1)	R/W
7:0	DI_601_VIAS[7:0]	ITU-R BT.601 Vertical Input Active Size	
0x0053		DI_FIELD601_TH (Default: 0 x 46)	R/W
7:0	FIELD601_TH	ITU-R BT.601 Internal Field Threshold	
0x01C0		DI_H_TOTAL_h	RO
7:3		Reserved	
2:0	DI_HOTS[10:8]	Horizontal Output Total Size	
0x01C1		DI_H_TOTAL_I	RO
7:0	DI_HOTS[7:0]	Horizontal Output Total Size	
0x01C2		DI_V_TOTAL_h	RO
7:3		Reserved	
2:0	DI_VOTS[10:8]	Vertical Output Total Size	
0x01C3		DI_V_TOTAL_I	RO
7:0	DI_VOTS[7:0]	Vertical Output Total Size	
0x01C4		DI_HOA_STR_h	RO
7:3		Reserved	
2:0	DI_HOA_STR[10:8]	Horizontal Output Active Start Point	
0x01C5		DI_HOA_STR_I	RO
7:0	DI_HOA_STR[7:0]	Horizontal Output Active Start Point	
0x01C6		DI_HOA_END_h	RO
7:3		Reserved	
2:0	DI_HOA_END[10:8]	Horizontal Output Active End Point	
0x01C7		DI_HOA_END_I	RO
7:0	DI_HOA_END[7:0]	Horizontal Output Active End Point	

0x01C8		DI_VOA_STR_h	RO
7:3		Reserved	
2:0	DI_VOA_STR[10:8]	Vertical Output Active Start Point	

0x01C9		DI_VOA_STR_I	RO
7:0	DI_VOA_STR[7:0]	Vertical Output Active Start Point	

0x01CA		DI_VOA_END_h	RO
7:3		Reserved	
2:0	DI_VOA_END[10:8]	Vertical Output Active End Point	

0x01CB		DI_VOA_END_I	RO
7:0	DI_VOA_END[7:0]	Vertical Output Active End Point	

6.4 IMAGE SCALING CONTROL REGISTERS

Bits	Register Name	Function	
	0x0061	SCALER_IVZOOM_h (Default: 0 x 02)	R/W
7:4		Reserved	
3:0	IVZOOM[19:16]	Inversed Vertical Zoom Ratio (= VIAS/VOAS)	

	0x0062	SCALER_IVZOOM_m (Default: 0 x 00)	R/W
7:0	IVZOOM[15:8]	Inversed Vertical Zoom Ratio (= VIAS/VOAS)	

	0x0063	SCALER_IVZOOM_l (Default: 0 x 00)	R/W
7:0	IVZOOM[7:0]	Inversed Vertical Zoom Ratio (= VIAS/VOAS)	

	0x0065	SCALER_IHZOOM_h (Default: 0 x 02)	R/W
7:4		Reserved	
3:0	IHZOOM[19:16]	Inversed Horizontal Zoom Ratio (= HIAS/HOAS)	

	0x0066	SCALER_IHZOOM_m (Default: 0 x 00)	R/W
7:0	IHZOOM[15:8]	Inversed Horizontal Zoom Ratio (= HIAS/HOAS)	

	0x0067	SCALER_IHZOOM_l (Default: 0 x 00)	R/W
7:0	IHZOOM[7:0]	Inversed Horizontal Zoom Ratio (= HIAS/HOAS)	

	0x0068	SCALER_HSTR_OFFSET (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	HSTR_OFFSET	Sub-Pixel Horizontal Starting Point OFFset for Scaling - For Scale Down : $HSTR_OFFSET = [(HIAS-1) - (HOAS - 1) / Hratio] * 16$ - For Scale Up : $HSTR_OFFSET = 32 - [16 * \{ (2 * \lceil 3*HOAS/HIAS \rceil + HOAS - 1) / Hratio - HIAS - 1 \}] \% 32$	

0x0069		SCALER_VSTR_OFFSET (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	VSTR_OFFSET	Sub-Pixel Vertical Starting Point OFFset for Scaling - For Scale Down : $VSTR_OFFSET = [(VIAS-1) - (VOAS - 1) / Vratio] * 16$ - For Scale Up : $VSTR_OFFSET = 32 - [16 * \{2 * [3*VOAS/VIAS - 1] + VOAS - 1\} / Vratio - VIAS - 1] \% 32$	

6.5 ADVANCED COLOR CONTRAST ENHANCEMENT (ACE) CONTROL REGISTERS

Bits	Register Name	Function
	0x0070	BU_H_START_h (Default: 0 x 00) R/W
7:3		Reserved
2:0	BU_HSP[10:8]	BOOST UP AREA : Horizontal Start Point

	0x0071	BU_H_START_I (Default: 0 x 00) R/W
7:0	BU_HSP[7:0]	BOOST UP AREA : Horizontal Start Point

	0x0072	BU_V_START_h (Default: 0 x 00) R/W
7:3		Reserved
2:0	BU_VSP [10:8]	BOOST UP AREA : Vertical Start Point

	0x0073	BU_V_START_I (Default: 0 x 00) R/W
7:0	BU_VSP[7:0]	BOOST UP AREA : Vertical Start Point

	0x0074	BU_H_END_h (Default: 0 x 00) R/W
7:3		Reserved
2:0	BU_HEP[10:8]	BOOST UP AREA : Horizontal End Point

	0x0075	BU_H_END_I (Default: 0 x 00) R/W
7:0	BU_HEP[7:0]	BOOST UP AREA : Horizontal End Point

	0x0076	BU_V_END_h (Default: 0 x 00) R/W
7:3		Reserved
2:0	BU_VEP[10:8]	BOOST UP AREA : Vertical End Point

	0x0077	BU_V_END_I (Default: 0 x 00) R/W
7:0	BU_VEP[7:0]	BOOST UP AREA : Vertical End Point - BU_H/V_Start/End Point is changed when BU_VEP[7:0] is controlled.

0x0078		BU_SUB_H_START_h (Default: 0 x 00)	R/W
7	SUB_ZONESEL	if (SUB_ZONESEL == 1) then BU_SUB_HSP = BU_HSP, BU_SUB_VSP = BU_VSP, BU_SUB_HEP = BU_HEP, BU_SUB_VEP = BU_VEP;	
6:3		Reserved	
2:0	BU_SUB_HSP[10:8]	BOOST UP Calculating AREA : Horizontal Start Point	

0x0079		BU_SUB_H_START_I (Default: 0 x 00)	R/W
7:0	BU_SUB_HSP [7:0]	BOOST UP Calculating AREA : Horizontal Start Point	

0x007A		BU_SUB_V_START_h (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	BU_SUB_VSP [10:8]	BOOST UP Calculating AREA : Vertical Start Point	

0x007B		BU_SUB_V_START_I (Default: 0 x 00)	R/W
7:0	BU_SUB_VSP [7:0]	BOOST UP Calculating AREA : Vertical Start Point	

0x007C		BU_SUB_H_END_h (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	BU_SUB_HEP [10:8]	BOOST UP Calculating AREA : Horizontal End Point	

0x007D		BU_SUB_H_END_I (Default: 0 x 00)	R/W
7:0	BU_SUB_HEP [7:0]	BOOST UP Calculating AREA : Horizontal End Point	

0x007E		BU_SUB_V_END_h (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	BU_SUB_VEP [10:8]	BOOST UP Calculating AREA : Vertical End Point	

0x007F		BU_SUB_V_END_I (Default: 0 x 00)	R/W
7:0	BU_SUB_VEP [7:0]	BOOST UP Calculating AREA : Vertical End Point - BU_SUB_H/V_Start/End Point is changed when BU_SUB_VEP[7:0] is controlled	

0x0080		BU_MAX_COEF (Default: 0 x 00)	R/W
7:0	MAX_coeff	Response time to MAX	

0x0081		BU_MIN_COEF (Default: 0 x 00)	R/W
7:0	MIN_coeff	Response time to MIN	

0x0082		BU_AVR_L1_COEF (Default: 0 x 00)	R/W
7:0	AVR_L1_coeff	AVR Response time before stretching	

0x0083		BU_AVR_COEF (Default: 0 x 00)	R/W
7:0	AVR_coeff	AVR Response time after stretching	

0x0084		BU_MAX_THRESHOLD (Default: 0 x 00)	R/W
7:4	Ymax_HIGH_int	Upper threshold for MAX : Ymax_HIGH_TH >= MAX >= Ymax_LOW_TH	
3:0	Ymax_LOW_int	Lower threshold for MAX	

0x0085		BU_MIN_THRESHOLD (Default: 0 x 00)	R/W
7:4	Ymin_HIGH_int	Upper threshold for MIN : Ymin_HIGH_TH >= MIN >= Ymin_LOW_TH	
3:0	Ymin_LOW_int	Lower threshold for MIN	

0x0086		BU_MAX_1ST (Default: 0 x 00)	R/W
7:0	Ymax_1st_base	The number of pixels considered as the biggest value in MAX	

0x0086		BU_MAX_1ST (Default: 0 x 00)	R/W
7:0	Ymax_1st_base	The number of pixels considered as the biggest value in MAX	

0x0087		BU_MAX_2ND (Default: 0 x 00)	R/W
7:0	Ymax_2nd_base	The number of pixels considered as the next biggest value in MAX When Ymax_1st_base condition is not met.	

0x0088		BU_MIN_1ST (Default: 0 x 00)	R/W
7:0	Ymin_1st_base	The number of pixels considered as the smallest value in MIN	

0x0089		BU_MIN_2 ND (Default: 0 x 00)	R/W
7:0	Ymin_2nd_base	The number of pixels considered as the next smallest value in MIN When Ymin_1 st _base condition is not met.	

0x008A		BU_AVR_L1_H (Default: 0 x 00)	R/W
7:0	AVR_L1_H	Adjusts the MAX value.	

0x008B		BU_AVR_L1_L (Default: 0 x 00)	R/W
7:0	AVR_L1_L	Adjusts the MIN value.	

0x008C		BU_LEVEL (Default: 0 x 00)	R/W
7	BOOST_ON	ON / OFF (1: ON) of stretching and boost	
6:1		Reserved	
0	ST_LEVEL	Stretching Level (0: Low Stretch, 1: High Stretch)	

0x008D		BU_MINMAX_CONTROL (Default: 0 x 00)	R/W
7:5		Reserved	
4	Ymax_Ctrl	The method of modifying MAX : (M_MAX) 0 : Not Stretching 1 : M_MAX = 1/8 * MAX	
3:1		Reserved	
0	Ymin_Ctrl	The method of modifying Min : (M_MIN) 0 : Not Stretching 1 : M_MIN = 1/8 * MIN	

0x008E		BU_AVR_LUT_GAIN (Default: 0 x 00)	R/W
7:2		Reserved	
1:0	AVR_LUT_Gain	Boost gain control by AVR and LUT	

0x0090		BU_COLOR_CONTROL (Default: 0 x 00)	R/W
7:6		Reserved	
5	ITU-R.SEL	ITU-R BT.656 OFFset correction ON / OFF (1: ON)	
4:2	RGBrate	Color correction rate (0.5625, 0.625, 0.6875, 0.75, 0.8125, 0.875, 0.9375, 1)	
1:0	SEL_div	Selects the color correction method 0 : OFF 1 : Color correction coefficient determining filter 1 2 : Color correction coefficient determining filter 2 3 : Color correction coefficient determining filter 3	

0x0091		BU_APERTURE_GAIN (Default: 0 x 00)	R/W
7:4		Reserved	
3:0	AP_GAIN	Sharpness Gain Control	

0x0094		BU_GRAPH_CONTROL (Default: 0 x 00)	R/W
7:2		Reserved	
1	GR_MODE	BOOST UP LUT Graph ON / OFF (1: ON)	
0	GR_STYLE	BOOST UP LUT Graph Style Select (1: Bar, 0: Line)	

0x0095		BU_AVR_RATE_h (Default: 0 x 00)	R/W
7:1		Reserved	
0	AVRrate[8]	Adjusts boost rate (No boost if the bit is 0.)	

0x0096		BU_AVR_RATE_l (Default: 0 x 00)	R/W
7:0	AVRrate[7:0]	Adjusts boost rate (No boost if the bit is 0.) AVRrate[8:0] binary number. Only the first 1 bit is constant. For example, 9bits is expressed as X.xxxxxxxx. The minimum must be 0.5.	

0x0097		BU_FILTER_CONTROL (Default: 0 x 00)	R/W
7:6		Reserved	
5	AREA_ON	Boost border line including screen outer line (1: ON, 0: OFF)	
4:0		Reserved	

6.6 GLOBAL IMAGE GAIN & OFFSET CONTROL REGISTER

Bits	Register Name	Function	
0x00D0		CONTRAST_CONTROL_TYPE (Default: 0 x 01F)	R/W
7:6		Reserved	
5:4	CONT_TYPE	Determines magnification of the contrast control area 00: 0 ~ 0.99609375, 01: 0.5 ~ 1.49609375 (Default) 10: 0 ~ 1.9921875, 11: 0 ~ 3.984375	
3	ZONE_CT	Zone area control type 1: Adjusts global/zone together based on global (Default) 0: Adjusts global/zone separately	
2	BLACK_CT	Black level control type 1: Adjusts R/G/B together based on R (Default) 0: Adjusts R/G/B separately	
1	CONT_CT	Contrast control type 1: Adjusts R/G/B together based on R (Default) 0: Adjusts R/G/B separately	
0	BRIGHT_CT	Brightness control type 1: Adjusts R/G/B together based on R (Default) 0: Adjusts R/G/B separately	

0x00D1		CONTRAST_R_BLACK_global (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	R_BLACK_global	Adjusts R channel Black level. R/G/B are adjusted separately if BLACK_CT (ADDR 0x00D0[2]) is 0, and are adjusted together based on R if it is 1.	

0x00D2		CONTRAST_G_BLACK_global (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	G_BLACK_global	Adjusts G channel Black level. R/G/B are adjusted separately if BLACK_CT (ADDR 0x00D0[2]) is 0, and are adjusted together based on R if it is 1.	

0x00D3		CONTRAST_B_BLACK_global (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	B_BLACK_global	Adjusts B channel Black level. R/G/B are adjusted separately if BLACK_CT (ADDR 0x00D0[2]) is 0, and are adjusted together based on R if it is 1.	

0x00D4		CONTRAST_R_CONT_global (Default: 0 x 80)	R/W
7:0	R_CONT_global	Adjusts R channel Contrast. R/G/B are adjusted separately if CONT_CT(ADDR 0x00D0[1]) is 0, and are adjusted together based on R if it is 1.	

0x00D5		CONTRAST_G_CONT_global (Default: 0 x 80)	R/W
7:0	G_CONT_global	Adjusts G channel Contrast. R/G/B are adjusted separately if CONT_CT(ADDR 0x00D0[1]) is 0, and are adjusted together based on R if it is 1.	

0x00D6		CONTRAST_B_CONT_global (Default: 0 x 80)	R/W
7:0	B_CONT_global	Adjusts B channel Contrast. R/G/B are adjusted separately if CONT_CT(ADDR 0x00D0[1]) is 0, and are adjusted together based on R if it is 1.	

0x00D7		CONTRAST_R_BRIGHT_global (Default: 0 x 00)	R/W
7:0	R_BRIGHT_global	Adjusts R channel Brightness. R/G/B are adjusted separately if BRIGHT_CT(ADDR 0x00D0[0]) is 0, and are adjusted together based on R if it is 1.	

0x00D8		CONTRAST_G_BRIGHT_global (Default: 0 x 00)	R/W
7:0	G_BRIGHT_global	Adjusts G channel Brightness. R/G/B are adjusted separately if BRIGHT_CT (ADDR 0x00D0[0]) is 0, and are adjusted together based on R if it is 1.	

0x00D9		CONTRAST_B_BRIGHT_global (Default: 0 x 00)	R/W
7:0	B_BRIGHT_global	Adjusts B channel Brightness. R/G/B are adjusted separately if BRIGHT_CT (ADDR 0x00D0[0]) is 0, and are adjusted together based on R if it is 1.	

0x00DA		CONTRAST_B_BLACK_ZONE (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	R_BLACK_ZONE	Adjusts R channel Black level in the boot area	

0x00DB		CONTRAST_B_BLACK_ZONE (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	G_BLACK_ZONE	Adjusts G channel Black level in the boot area	

0x00DC		CONTRAST_B_BLACK_ZONE (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	B_BLACK_ZONE	Adjusts B channel Black level in the boot area	

0x00DD		CONTRAST_R_CONT_ZONE (Default: 0 x 80)	R/W
7:0	R_CONT_ZONE	Adjusts R channel Contrast in the boot area	

0x00DE		CONTRAST_G_CONT_ZONE (Default: 0 x 80)	R/W
7:0	G_CONT_ZONE	Adjusts G channel Contrast in the boot area	

0x00DF		CONTRAST_B_CONT_ZONE (Default: 0 x 80)	R/W
7:0	B_CONT_ZONE	Adjusts B channel Contrast in the boot area	

0x00E0		CONTRAST_R_BRIGHT_ZONE (Default: 0 x 00)	R/W
7:0	R_BRIGHT_ZONE	Adjusts R channel Brightness in the boot area	

0x00E1		CONTRAST_G_BRIGHT_ZONE (Default: 0 x 00)	R/W
7:0	G_BRIGHT_ZONE	Adjusts G channel Brightness in the boot area	

0x00E2		CONTRAST_B_BRIGHT_ZONE (Default: 0 x 00)	R/W
7:0	B_BRIGHT_ZONE	Adjusts B channel Brightness in the boot area	

0x00E3		CONTRAST_BG_COLOR_R (Default: 0 x 00)	R/W
7:6		Reserved	
5	BG_COLOR	Enable Background Color (1: ON, 0: OFF) - Background Color correspond to BG_COLOR_R,G,B color pallet - Highest priority in color control.	
4:0	BG_COLOR_R	R Channel Background Color	

0x00E4		CONTRAST_BG_COLOR_G (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	BG_COLOR_G	G Channel Background Color	

0x00E5		CONTRAST_BG_COLOR_B (Default: 0 x 10)	R/W
7:5		Reserved	
4:0	BG_COLOR_B	B Channel Background Color	

6.7 OSD CONTROL REGISTERS

Bits	Register Name	Function
0x0100		OSD_CHAR_TONE (Default: 0 x 60) R/W
7	OSD_EN	OSD Output Enable (1: Enable, 0: Disable)
6	DSRAM_CLRN	DSRAM Clear (1: No Operation, 0: Active)
5	FTRAM_CLRN	FONT RAM Clear (1: No Operation, 0: Active)
4	ITENSITY	INTENSITY Select
3	CH_TONE	Character half Toning : if (OSD_TONE[2] == 0 && OSD_TONE[1:0] != 0 && CH_TONE == 1) then If Half Tone (Transparency) is enabled, it is applied to the font area.
2:0	OSD_TONE	OSD half Toning : 0: OSD bypass and input image are expressed. (Default) 1: Input Image and OSD are mixed at the rate of 0.25. 2: Input Image and OSD are mixed at the rate of 0.5. 3: Input Image and OSD are mixed at the rate of 0.75. 4 or higher : Only OSD is expressed without mixing with the input image.

0x0101		OSD_FONT_SIZE (Default: 0 x 00) R/W
7:6	CH_HSZ	Determines, based on the font size (12 × 18), the magnifying rate of the character horizontal size. - For example, if CH_HSZ is set to 1, the horizontal size of the character becomes 12 × 2 Pixel. (00: 12 × 1, 01: 12 × 2, 10: 12 × 3, 11: 12 × 4)
5:4	CH_VSZ	Determines, based on the font size (12 × 18), the magnifying rate of the character vertical size. - For example, if CH_VSZ is set to 3, the vertical size of the character becomes 18 × 4 Pixel. (00: 18 × 1, 01: 18 × 2, 10: 18 × 3, 11: 18 × 4)
3:0	ROW_SP	Controls the number of row spaces between the upper and lower fonts. The row space is expressed in interworking with vertical pixels in accordance with the character vertical size. - For example, if ROW_SP is 2 and CH_VSZ is 2, the row space is 6 lines.

0x0102		OSD_HFONT (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	OSD_HFONT	The number of horizontal fonts of OSD - If OSD_HFONT is 30, the number of horizontal fonts of OSD is 30.	

0x0103		OSD_VFONT (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	OSD_VFONT	The number of vertical fonts of OSD. - If OSD_VFONT is 15, the number of vertical fonts of OSD is 15.	

0x0104		OSD_HSP_h (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	OSD_HSP[10:8]	Sets the horizontal start point of OSD. - If W_BDSH_EN is 1, and if OSD_HSP is lower than 6 as W_BDSH is 1, OSD_HSP is 6.	

0x0105		OSD_HSP_I (Default: 0 x 00)	R/W
7:0	OSD_HSP[7:0]	Sets the horizontal start point of OSD.	

0x0106		OSD_VSP_h (Default: 0 x 00)	R/W
7:3		Reserved	
2:0	OSD_VSP[10:8]	Sets Vertical Start Point of OSD. - If W_BDSH_EN is 1, and OSD_VSP is lower than 6 as W_BDSH is 1, OSD_VSP is 6.	

0x0107		OSD_VSP_I (Default: 0 x 00)	R/W
7:0	OSD_VSP[7:0]	Sets the vertical start point of OSD.	

0x0108		OSD_BORDER_SHADOW (Default: 0 x 00)	R/W
7:5		Reserved	
4	W_BDSH_EN	Controls OSD Main Window Border / Shadow Enable 1: Enables OSD Main Window Border / shadow 0: OSD Main Window Border / shadow is disappeared regardless of W_BDSH	
3	W_BDSH	Border and shadow of OSD window is determined by setting W_BDSH to 0 or 1 as W_BDSH_EN(ADDR 0x0108[4]) is 1. (1: OSD Main Window Bordering, 0: OSD Main Window Shadow)	
2	MW_BDSH_EN	Controls border / shadow enable of multiple windows. 1: Enables OSD Multiple Windows Border / shadow 0: Multiple Window Border / shadow is disappeared regardless of MW_BDSH	
1	MW_BDSH	Border and shadow of OSD window is determined by setting MW_BDSH to 0 or 1 as MW_BDSH_EN(ADDR 0x0108[2]) is 1. (1: OSD Multiple Window Bordering, 0: OSD Multiple Window Shadow)	
0	CH_BDSH_EN	Controls Character Border/Shadow Enable 1: Character border if DSRAM[15] is 1, and Character shadow if 0 0: Border / Shadow are disabled regardless of DSRAM[15].	

0x0109		OSD_MW_ENABLE (Default: 0 x 00)	R/W
7:4		Reserved	
3	W1_EN	Multiple Windows 1 Enable Control 1: LUT color of W1C is expressed in Multiple Windows 1 0: Multiple windows 1 is disabled.	
2	W2_EN	Multiple Windows 2 Enable Control. 1: LUT color of W2C is expressed in Multiple Windows 2 0: Multiple windows 2 is disabled.	
1	W3_EN	Multiple Windows 3 Enable Control. 1: LUT color of W3C is expressed in Multiple Windows 3 0: Multiple windows 3 is disabled.	
0	W4_EN	Multiple Windows 4 Enable Control. 1: LUT color of W4C is expressed in Multiple Windows 4 0: Multiple windows 4 is disabled.	

0x010A		OSD_MW_PRIORITY (Default: 0 x 00)	R/W
7:6	W1_PRT	Sets priority of W1 in 4 Multiple Windows - The priority order is W1, W2, W3 and W4 if the same priority is given. (0: Highest Priority, 1: 2nd Priority, 2: 3rd Priority, 2: 4th Priority)	
5:4	W2_PRT	Sets priority of W2 in 4 Multiple Windows - The priority order is W1, W2, W3 and W4 if the same priority is given. (0: Highest Priority, 1: 2nd Priority, 2: 3rd Priority, 2: 4th Priority)	
3:2	W3_PRT	Sets priority of W3 in 4 Multiple Windows - The priority order is W1, W2, W3 and W4 if the same priority is given. (0: Highest Priority, 1: 2nd Priority, 2: 3rd Priority, 2: 4th Priority)	
1:0	W4_PRT	Sets priority of W4 in 4 Multiple Windows - The priority order is W1, W2, W3 and W4 if the same priority is given. (0: Highest Priority, 1: 2nd Priority, 2: 3rd Priority, 2: 4th Priority)	

0x010B		OSD_BDSH_COLOR (Default: 0 x 00)	R/W
7:6		Reserved	
5:4	WSH_C	Selects shadow color of OSD Main/ Multiple windows 0: LUT12[3:0] is applied to Windows Shadow Color 1: LUT13[3:0] is applied to Windows Shadow Color 2: LUT14[3:0] is applied to Windows Shadow Color 3: LUT15[3:0] is applied to Windows Shadow Color	
3:0	CH_BSC	Selects Character Border / Shadow Color as CH_BDSH_EN (ADDR 0x0108[0] is 1. You can select from LUT0 to LUT15 in this way. 0: LUT0[7:4] is used as the Border / Shadow Color of the character 1: LUT1[7:4] is used as Border / Shadow Color of the character 2: LUT2[7:4] is used as Border / Shadow Color of the character 3: LUT3[7:4] is used as Border / Shadow Color of the character	

0x010C		OSD_SHADOW_SIZE_MCF (Default: 0 x 00)	R/W
7:6		Reserved	
5:4	WSH_SZ	<p>Controls the window shadow size as W_BDSH_EN (ADDR 0x0108[4]) is 1 and W_BDSH(ADDR 0x0108[3]) is 0.</p> <p>0. Horizontal/vertical shadow size of the OSD main window is 1 pixel in both horizontal and vertical.</p> <p>1. Horizontal/vertical shadow size of the OSD main window is 2 pixel in both horizontal and vertical.</p> <p>2. Horizontal/vertical shadow size of the OSD main window is 3 pixel in both horizontal and vertical.</p> <p>3. Horizontal/vertical shadow size of the OSD main window is 4 pixel in both horizontal and vertical.</p> <p>Controls the window shadow size as MW_BDSH_EN (ADDR 0x0108[2]) is 1 and MW_BDSH(ADDR 0x0108[1]) is 0.</p> <p>Horizontal/vertical shadow size of the multiple windows are the same as OSD main window.</p>	
3:0	N_MCF	<p>Number of Multi-Colored RAM Font</p> <p>- Up to 9 multi color fonts are available out of 28 RAM fonts. When considering R/G/B, Up to 27 fonts (9x3) are available, and single color font is used for the remaining 1 font. If 4 MCFs are used, 4*3 = 12 fonts out of 28 RAM fonts are used for MCF, and remaining 16 fonts can be used for SF.</p>	

0x010D		OSD_BLINK_CONTROL (Default: 0 x 00)	R/W
7:5		Reserved	
4:2	BLNK_SEL	<p>Blink duty Select:</p> <p>0: OFF 32 Frame (about 0.5sec) / ON 32 Frame (about 0.5sec)</p> <p>1: OFF 64 Frame (about 1sec) / ON 32 Frame (about 0.5sec)</p> <p>2: OFF 32 Frame (about 0.5sec) / ON 64 Frame (about 1sec)</p> <p>3: OFF 64Frame (about 1sec) / ON 64 Frame (about 1sec)</p> <p>4: OFF 96 Frame (about 1.5sec) / ON 96Frame (about 1.5sec)</p> <p>5: OFF 128 Frame (about 2sec) / ON 64 Frame (about 1sec)</p> <p>6: OFF 64 Frame (about 1sec) / ON 128 Frame (about 2sec)</p> <p>7: OFF 128 Frame (about 2sec) / ON 128 Frame (about 2sec)</p>	
1	BL_NTRA	<p>Blink or No_Tone_Raster:</p> <p>1: If Display RAM[14] is 1, Blink according to BLNK_SEL</p> <p>0: If Display RAM[14] is 0, half tone is not applied to the raster part. In this case, border/shadow of character is disabled.</p>	
0	BLNK_C	<p>Blink Color inversion:</p> <p>1: If Blink is OFF, the complementary color of Raster is displayed in the character part.</p> <p>0: If Blink is OFF, the Raster color is displayed in the character part.</p>	

0x010E		OSD_W1_W2_COLOR (Default: 0 x 00)	R/W
7:4	W1C	Multiple Windows 1 Color. - If W1_EN (ADDR 0x0109[3]) is 1 and n(0~15) is selected for W1C, LUTn[3:0] is assigned for Multiple Windows 1. For example, if W1C is 7 then LUT7[3:0] is assigned for the color of windows multiple windows 1.	
3:0	W2C	Multiple Windows 2 Color. - If W2_EN (ADDR 0x0109[2]) is 1 and n(0~15) is selected for W2C, LUTn[3:0] is assigned for Multiple Windows 2.	

0x010F		OSD_W3_W4_COLOR (Default: 0 x 00)	R/W
7:4	W3C	Multiple Windows 3 Color. - If W3_EN (ADDR 0x0109[1]) is 1 and n(0~15) is selected for W3C, LUTn[3:0] is assigned for Multiple Windows 3.	
3:0	W4C	Multiple Windows 4 Color. - If W4_EN (ADDR 0x0109[0]) is 1 and n(0~15) is selected for W4C, LUTn[3:0] is assigned for Multiple Windows 4.	

0x0110		OSD_W1_ROW_STR (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W1R_STR	Row Start position (1(not 0) ~ 31) of Multiple Windows 1 - If the bit is 1, y of the start (x, y) of Multiple Windows 1 is 1	

0x0111		OSD_W1_ROW_END (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W1R_END	Row End position (1(not 0) ~ 31) of Multiple Windows 1 - If the bit is 2, y of the end (x, y) of Multiple Windows 1 is 2	

0x0112		OSD_W1_COLUMN_STR (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W1C_STR	Column Start position (1(not 0) ~ 63) of Multiple Windows 1 - If the bit is 1, x of the start (x, y) of Multiple Windows 1 is 1	

0x0113		OSD_W1_COLUMN_END (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W1C_END	Column End position (1(not 0) ~ 63) of Multiple Windows 1 - If the bit is 2, x of the end (x, y) of Multiple Windows 1 is 2	

0x0114		OSD_W2_ROW_STR (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W2R_STR	Row Start position (1(not 0) ~ 31) of Multiple Windows 2 - If the bit is 1, y of the start (x, y) of Multiple Windows 2 is 1	

0x0115		OSD_W2_ROW_END (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W2R_END	Row End position (1(not 0) ~ 31) of Multiple Windows 2 - If the bit is 2, y of the end (x, y) of Multiple Windows 2 is 2	

0x0116		OSD_W2_COLUMN_STR (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W2C_STR	Column Start position (1(not 0) ~ 63) of Multiple Windows 2 - If the bit is 1, x of the start (x, y) of Multiple Windows 2 is 1	

0x0117		OSD_W2_COLUMN_END (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W2C_END	Column End position (1(not 0) ~ 63) of Multiple Windows 2 - If the bit is 2, x of the end (x, y) of Multiple Windows 2 is 2	

0x0118		OSD_W3_ROW_STR (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W3R_STR	Row Start position (1(not 0) ~ 31) of Multiple Windows 3 - If the bit is 1, y of the start (x, y) of Multiple Windows 3 is 1	

0x0119		OSD_W3_ROW_END (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W3R_END	Row End position (1(not 0) ~ 31) of Multiple Windows 3 - If the bit is 2, y of the end (x, y) of Multiple Windows 3 is 2	

0x011A		OSD_W3_COLUMN_STR (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W3C_STR	Column Start position (1(not 0) ~ 63) of Multiple Windows 3 - If the bit is 1, x of the start (x, y) of Multiple Windows 3 is 1	

0x011B		OSD_W3_COLUMN_END (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W3C_END	Column End position (1(not 0) ~ 63) of Multiple Windows 3 - If the bit is 2, x of the start (x, y) of Multiple Windows 3 is 2	

0x011C		OSD_W4_ROW_STR (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W4R_STR	Row Start position (1(not 0) ~ 31) of Multiple Windows 4 - If the bit is 1, y of the start (x, y) of Multiple Windows 4 is 1	

0x011D		OSD_W4_ROW_END (Default: 0 x 00)	R/W
7:5		Reserved	
4:0	W4R_END	Row End position (1(not 0) ~ 31) of Multiple Windows 4 - If the bit is 2, y of the end (x, y) of Multiple Windows 4 is 2	

0x011E		OSD_W4_COLUMN_STR (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W4C_STR	Column Start position (1(not 0) ~ 63) of Multiple Windows 4 - If the bit is 1, x of the start (x, y) of Multiple Windows 4 is 1	

0x011F		OSD_W4_COLUMN_END (Default: 0 x 00)	R/W
7:6		Reserved	
5:0	W4C_END	Column End position (1(not 0) ~ 63) of Multiple Windows 4 - If the bit is 2, x of the end (x, y) of Multiple Windows 4 is 2	

0x0120		OSD_LUT0 (Default: 0 x 00)	R/W
7:0	LUT0	Look Up Table 0 (LUT0[7:4]: Font Character Color (7: R, 6: G, 5: G, 4: B) LUT0[3:0]: Raster Font Color (3: R, 2: G, 1: G, 0: B))	

0x0121		OSD_LUT1 (Default: 0 x 00)	R/W
7:0	LUT1	Look Up Table 1 (LUT1[7:4]: Font Character Color, LUT1[3:0]: Font Raster Color)	

0x0122		OSD_LUT2 (Default: 0 x 00)	R/W
7:0	LUT2	Look Up Table 2 (LUT2[7:4]: Font Character Color, LUT2[3:0]: Font Raster Color)	

0x0123		OSD_LUT3 (Default: 0 x 00)	R/W
7:0	LUT3	Look Up Table 3 (LUT3[7:4]: Font Character Color, LUT3[3:0]: Font Raster Color)	

0x0124		OSD_LUT4 (Default: 0 x 00)	R/W
7:0	LUT4	Look Up Table 4 (LUT4[7:4]: Font Character Color, LUT4[3:0]: Font Raster Color)	

0x0125		OSD_LUT5 (Default: 0 x 00)	R/W
7:0	LUT5	Look Up Table 5 (LUT5[7:4]: Font Character Color, LUT5[3:0]: Font Raster Color)	

0x0126		OSD_LUT6 (Default: 0 x 00)	R/W
7:0	LUT6	Look Up Table 6 (LUT6[7:4]: Font Character Color, LUT6[3:0]: Font Raster Color)	

0x0127		OSD_LUT7 (Default: 0 x 00)	R/W
7:0	LUT7	Look Up Table 7 (LUT7[7:4]: Font Character Color, LUT7[3:0]: Font Raster Color)	

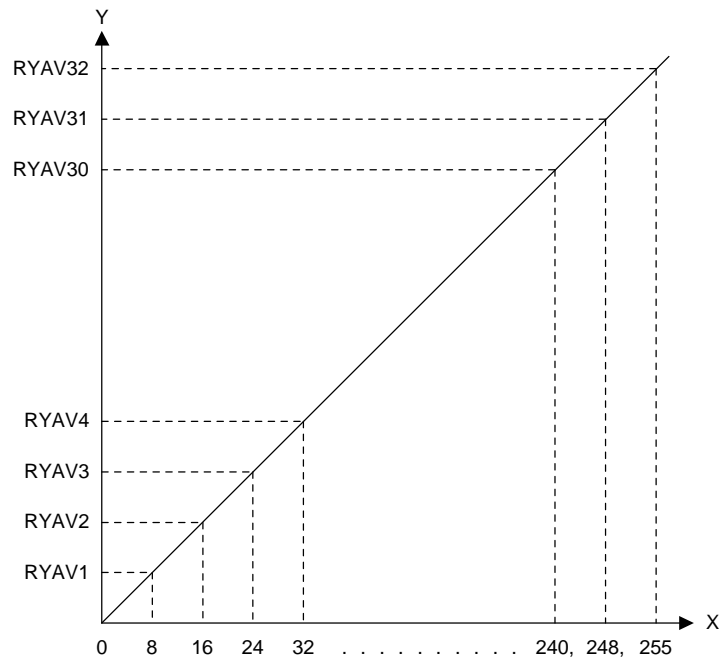
0x0128		OSD_LUT8 (Default: 0 x 00)	R/W
7:0	LUT8	Look Up Table 8 (LUT8[7:4]: Font Character Color, LUT8[3:0]: Font Raster Color)	

0x0129		OSD_LUT9 (Default: 0 x 00)	R/W
7:0	LUT9	Look Up Table 9 (LUT9[7:4]: Font Character Color, LUT9[3:0]: Font Raster Color)	

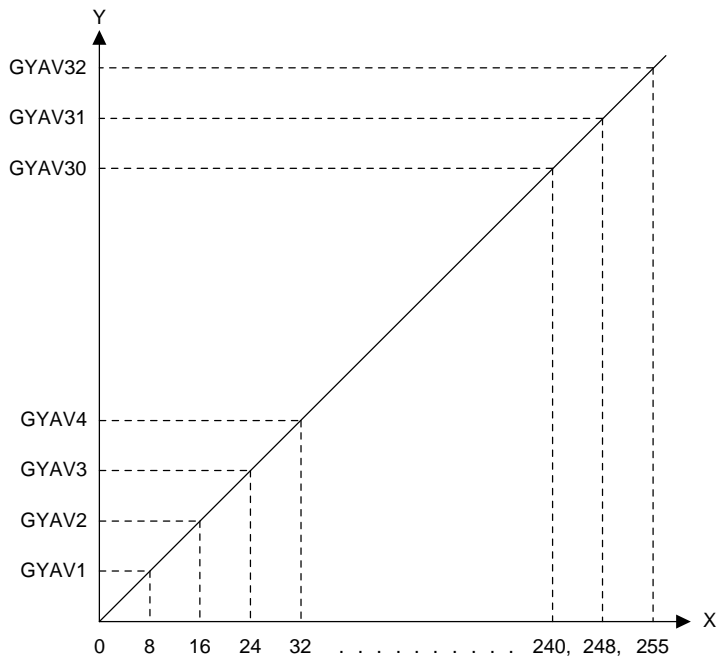
0x012A		OSD_LUT10 (Default: 0 x 00)	R/W
7:0	LUT10	Look Up Table 10 (LUT10[7:4]: Font Character Color, LUT10[3:0]: Font Raster Color)	
0x012B		OSD_LUT11 (Default: 0 x 00)	R/W
7:0	LUT11	Look Up Table 11 (LUT11[7:4]: Font Character Color, LUT11[3:0]: Font Raster Color)	
0x012C		OSD_LUT12 (Default: 0 x 00)	R/W
7:0	LUT12	Look Up Table 12 (LUT12[7:4]: Font Character Color, LUT12[3:0]: Font Raster Color)	
0x012D		OSD_LUT13 (Default: 0 x 00)	R/W
7:0	LUT13	Look Up Table 13 (LUT13[7:4]: Font Character Color, LUT13[3:0]: Font Raster Color)	
0x012E		OSD_LUT14 (Default: 0 x 00)	R/W
7:0	LUT14	Look Up Table 14 (LUT14[7:4]: Font Character Color, LUT14[3:0]: Font Raster Color)	
0x012F		OSD_LUT15 (Default: 0 x 00)	R/W
7:0	LUT15	Look Up Table 15 (LUT15[7:4]: Font Character Color, LUT15[3:0]: Font Raster Color)	
0x43EF		FONT_RAM_EN	R/W
7:6		Reserved	
0	FTRAM_EN	FONT RAM Enable (1: Enable, 0: Disable) Writes data on the FONT RAM, and enables it.	

6.8 GAMMA CORRECTION CONTROL REGISTER

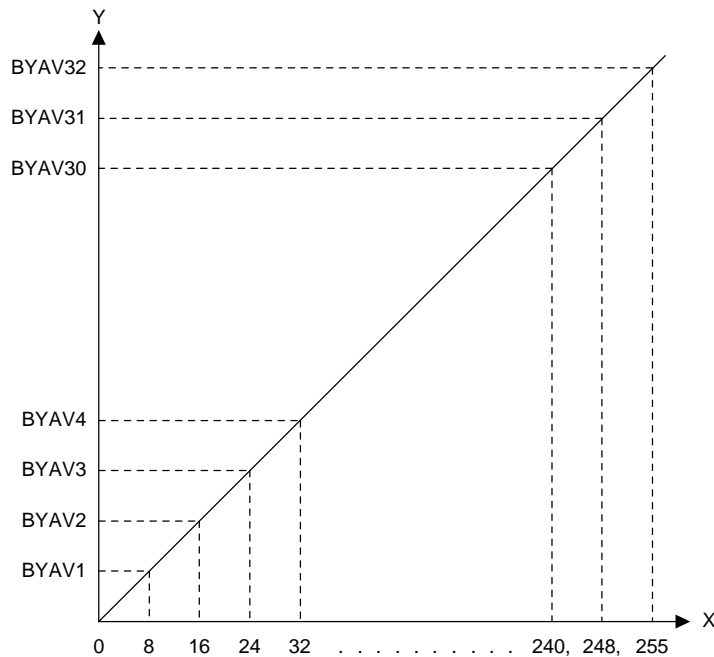
Bits	Register Name	Function	Default
0x0150		GAM_R_LUT_1_2	R/W
:		:	:
0x016F		GAM_R_LUT_31_32	R/W
7:0	RYAV1	RED Output (Y) Axis Value for Input (X) Axis Value 8, 16, 24, 32, . . . , 240, 248, 255	8'h08
7:0	RYAV2		8'h10
7:0	RYAV3		8'h18
7:0	RYAV4		8'h20
7:0	RYAV5		8'h28
7:0	RYAV6		8'h30
7:0	RYAV7		8'h38
7:0	RYAV8		8'h40
7:0	RYAV9		8'h48
7:0	RYAV10		8'h50
7:0	RYAV11		8'h58
7:0	RYAV12		8'h60
7:0	RYAV13		8'h68
7:0	RYAV14		8'h70
7:0	RYAV15		8'h78
7:0	RYAV16		8'h80
7:0	RYAV17		8'h88
7:0	RYAV18		8'h90
7:0	RYAV19		8'h98
7:0	RYAV20		8'hA0
7:0	RYAV21		8'hA8
7:0	RYAV22		8'hB0
7:0	RYAV23		8'hB8
7:0	RYAV24		8'hC0
7:0	RYAV25		8'hC8
7:0	RYAV26		8'hD0
7:0	RYAV27		8'hD8
7:0	RYAV28		8'hE0
7:0	RYAV29		8'hE8
7:0	RYAV30		8'hF0
7:0	RYAV31		8'hF8
7:0	RYAV32		8'hFF



Bits	Register Name	Function	Default
0x0170		GAM_G_LUT_1_2	R/W
:		:	:
0x018F		GAM_G_LUT_31_32	R/W
7:0	GYAV1	GREEN Output (Y) Axis Value for Input (X) Axis Value 8, 16, 24, 32, . . . , 240, 248, 255	8'h08
7:0	GYAV2		8'h10
7:0	GYAV3		8'h18
7:0	GYAV4		8'h20
7:0	GYAV5		8'h28
7:0	GYAV6		8'h30
7:0	GYAV7		8'h38
7:0	GYAV8		8'h40
7:0	GYAV9		8'h48
7:0	GYAV10		8'h50
7:0	GYAV11		8'h58
7:0	GYAV12		8'h60
7:0	GYAV13		8'h68
7:0	GYAV14		8'h70
7:0	GYAV15		8'h78
7:0	GYAV16		8'h80
7:0	GYAV17		8'h88
7:0	GYAV18		8'h90
7:0	GYAV19		8'h98
7:0	GYAV20		8'hA0
7:0	GYAV21		8'hA8
7:0	GYAV22		8'hB0
7:0	GYAV23		8'hB8
7:0	GYAV24		8'hC0
7:0	GYAV25		8'hC8
7:0	GYAV26		8'hD0
7:0	GYAV27		8'hD8
7:0	GYAV28		8'hE0
7:0	GYAV29		8'hE8
7:0	GYAV300		8'hF0
7:0	GYAV31		8'hF8
7:0	GYAV32		8'hFF



Bits	Register Name	Function	Default
0x0190		GAM_B_LUT_1_2	R/W
:		:	:
0x01AF		GAM_B_LUT_31_32	R/W
7:0	BYAV1	BLUE Output (Y) Axis Value for Input (X) Axis Value 8, 16, 24, 32, . . . , 240, 248, 255	8'h08
7:0	BYAV2		8'h10
7:0	BYAV3		8'h18
7:0	BYAV4		8'h20
7:0	BYAV5		8'h28
7:0	BYAV6		8'h30
7:0	BYAV7		8'h38
7:0	BYAV8		8'h40
7:0	BYAV9		8'h48
7:0	BYAV10		8'h50
7:0	BYAV11		8'h58
7:0	BYAV12		8'h60
7:0	BYAV13		8'h68
7:0	BYAV14		8'h70
7:0	BYAV15		8'h78
7:0	BYAV16		8'h80
7:0	BYAV17		8'h88
7:0	BYAV18		8'h90
7:0	BYAV19		8'h98
7:0	BYAV20		8'hA0
7:0	BYAV21		8'hA8
7:0	BYAV22		8'hB0
7:0	BYAV23		8'hB8
7:0	BYAV24		8'hC0
7:0	BYAV25		8'hC8
7:0	BYAV26		8'hD0
7:0	BYAV27		8'hD8
7:0	BYAV28		8'hE0
7:0	BYAV29		8'hE8
7:0	BYAV30		8'hF0
7:0	BYAV31		8'hF8
7:0	BYAV32		8'hFF



6.9 OSD RAM CONTROL REGISTERS

Address	Bits	Register Name	Function
0x1000 ~ 0x10FF	7:0	BU_LUT	ACCE Look Up Table
0x2000 ~ 0x2383	15:0	OSD_DSPRAM	Display RAM (450 × 16 bits) for OSD
0x3FFF ~ 0x43EE	11:0	OSD_FONTRAM	Font RAM for OSD, 28 Fonts (1Fonts = 18 × 12 bits)
0x43EF	0	FTRAM_EN	FONT RAM Enable (1: Enable, 0: Disable) Writes data on the FONT RAM, and enables it.

7 ELECTRICAL SPECIFICATION

7.1 ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Characteristics	Symbol	Rating		Unit
DC Supply Voltage	V_{DD}	1.8V V_{DD}	2.7	V
		3.3V V_{DD}	3.8	
DC Input Voltage	V_{IN}	3.3V input buffer	3.8	
		3.3V interface / 5V tolerant input buffer	6.5	
DC Output Voltage	V_{OUT}	3.3V output buffer	2.7	
		1.8V interface / 3.3V tolerant output buffer	3.8	
Latch Up Current	I_{Latch}	± 100		mA
Storage temperature	T_{STG}	Plastic	- 65 to 150	$^{\circ}C$

7.2 RECOMMENDED OPERATION CONDITIONS

Table 9. Recommended Operating Conditions

Characteristics	Symbol	Rating		Unit
DC Supply Voltage	V_{DD}	1.8V V_{DD}	1.8 ± 0.15	V
		3.3V V_{DD}	3.3 ± 0.3	
DC Input Voltage	V_{IN}	3.3V input buffer	3.3 ± 0.3	
		3.3V interface / 5V tolerant input buffer	3.0 ~ 5.25	
DC Output Voltage	V_{OUT}	3.3V output buffer	3.3 ± 0.3	
		1.8V interface / 3.3V tolerant output buffer	1.8 ± 0.15	
Operating Temperature	T_A	Commercial	0 to 70	$^{\circ}C$

7.3 DC ELECTRICAL CHARACTERISTICS

VDD1 = 3.3V ± 0.3V, VDD2 = VDDA = 1.8V ± 0.15V, TA = 25°C

Table 10. DC Electrical Characteristics at 3.3V

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark	
Supply Voltage	Digital Power 1	V_{DD}	V_{DD1}	3.0	3.3	3.6	V	*1	
	Digital Power 2		V_{DD2}	1.65	1.8	1.95	V	*2	
	Analog Power		V_{DDA}	1.65	1.8	1.95	V	*3	
Input Voltage	High Level	V_{IH}		2.0			V	*4	
	Low Level	V_{IL}				0.8	V		
Output Voltage	High Level	V_{OH}	$I_{OH} = -2mA$	2.4			V	*5	
			$I_{OH} = -4mA$	2.4			V	*6	
			$I_{OH} = -20mA$	2.4			V	*7	
	Low Level	V_{OL}	$I_{OL} = 2mA$			0.4	V	*5	
			$I_{OL} = 4mA$			0.4	V	*6	
			$I_{OL} = 20mA$			0.4	V	*7	
Schmitt Trigger	Positive-going threshold	V_{T+}	CMOS			2.0	V	*8	
	Negative-going threshold	V_{T-}	CMOS	0.8			V		
Input Current	High Level	Input buffer	I_{IH}	$V_{IN} = V_{DD}$	-10		10	μA	*9
	Level				Input buffer with Pull-down	10	33	60	μA
	Low Level	Input buffer	I_{IL}	$V_{IN} = V_{SS}$	-10		10	μA	*9
Tri-state Output Leakage Current		I_{OZ}	$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	μA	*11	
Power Consumption		P_d				900	mW		

[Remark]

*1 : Pin 10, 39, 76

*2 : Pin 21, 57, 94

*3 : Pin 15, 19

*4 : All Input Pins

*5 : Pin 58, 59, 60

*6 : Pin 1~2, 8, 31~38, 40~47, 49~56, 73~75, 77~84, 86~93, 95~100

*7 : Pin 72

*8 : Pin 6~9, 61~65

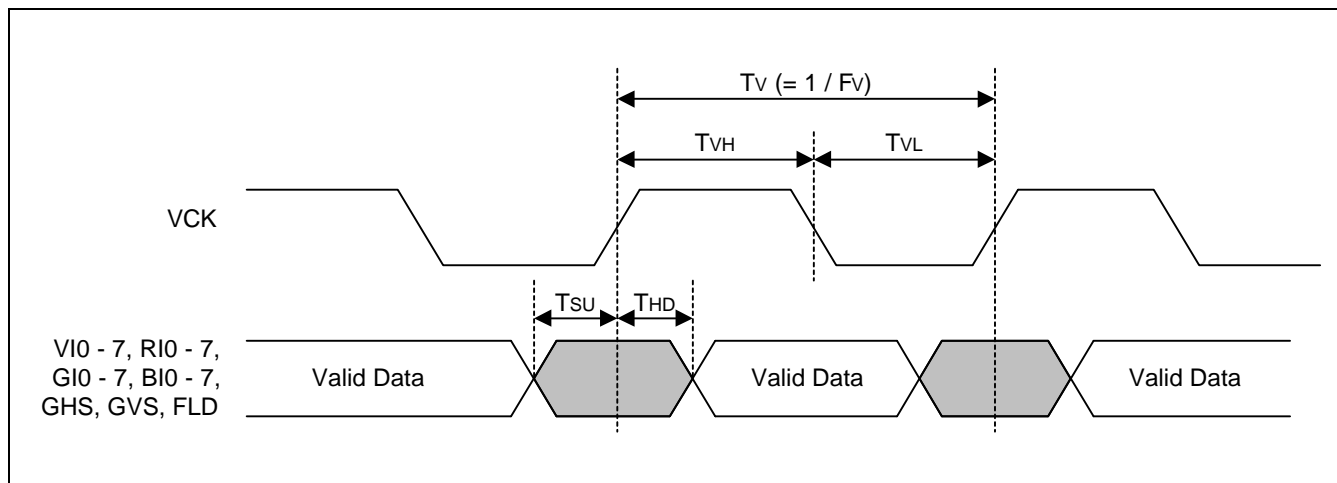
*9 : Pin 6~9, 11, 20, 22~29, 61~65, 67~68

*10 : Pin 4~5, 31~38, 40~47, 49~56, 69~71

*11 : Pin 1~2, 31~38, 40~47, 49~56, 77~84, 86~93, 95~100

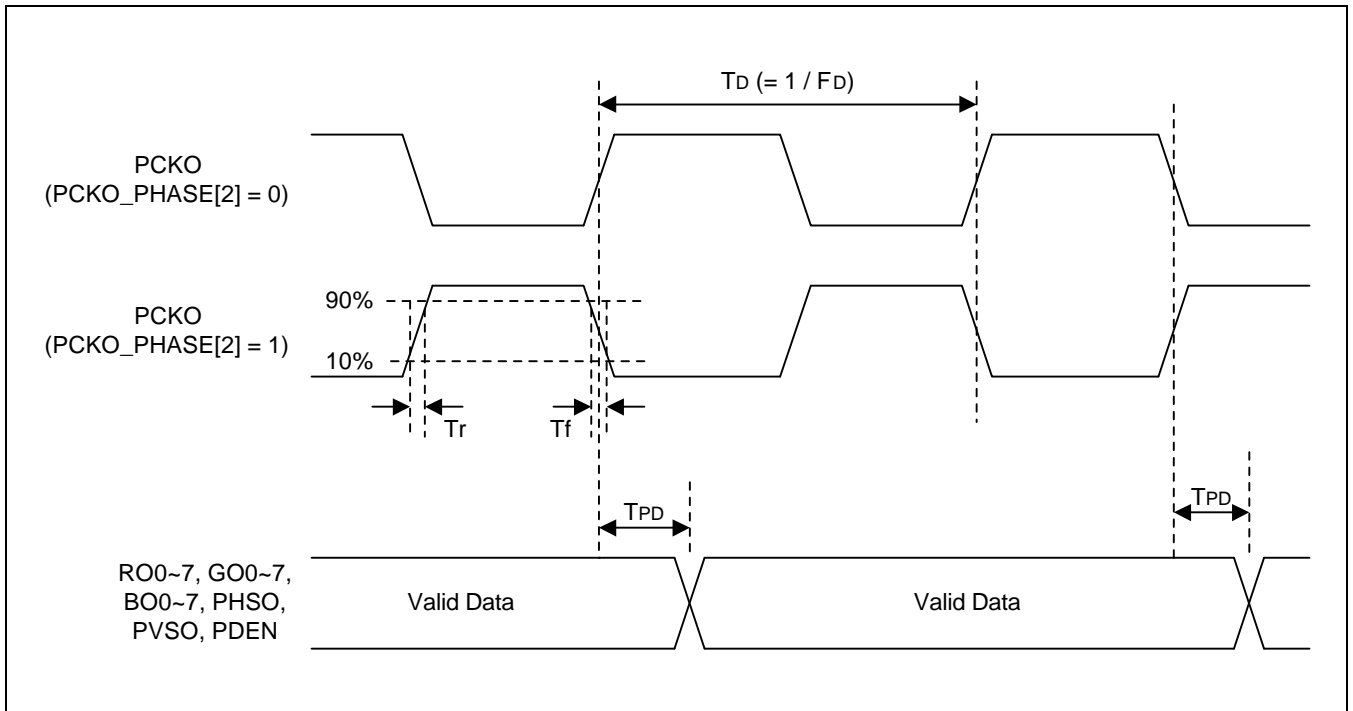
7.4 AC ELECTRICAL CHARACTERISTICS

7.4.1 Video Input Timing Characteristics



Item	Symbol	Min	Typ	Max	Units
Setup Time to VCK, input VI0~7, RIO0~7, GIO0~7, BIO0~7, GHS, GVS, FLD	T_{SV}	2.0			ns
Hold Time to VCK, input VI0~7, RIO0~7, GIO0~7, BIO0~7, GHS, GVS, FLD	T_{HD}	2.0			ns
Input Frequency	F_V			90	MHz
Input High Duration Time	T_{VH}	3.0			ns
Input Low Duration Time	T_{VL}	3.0			ns

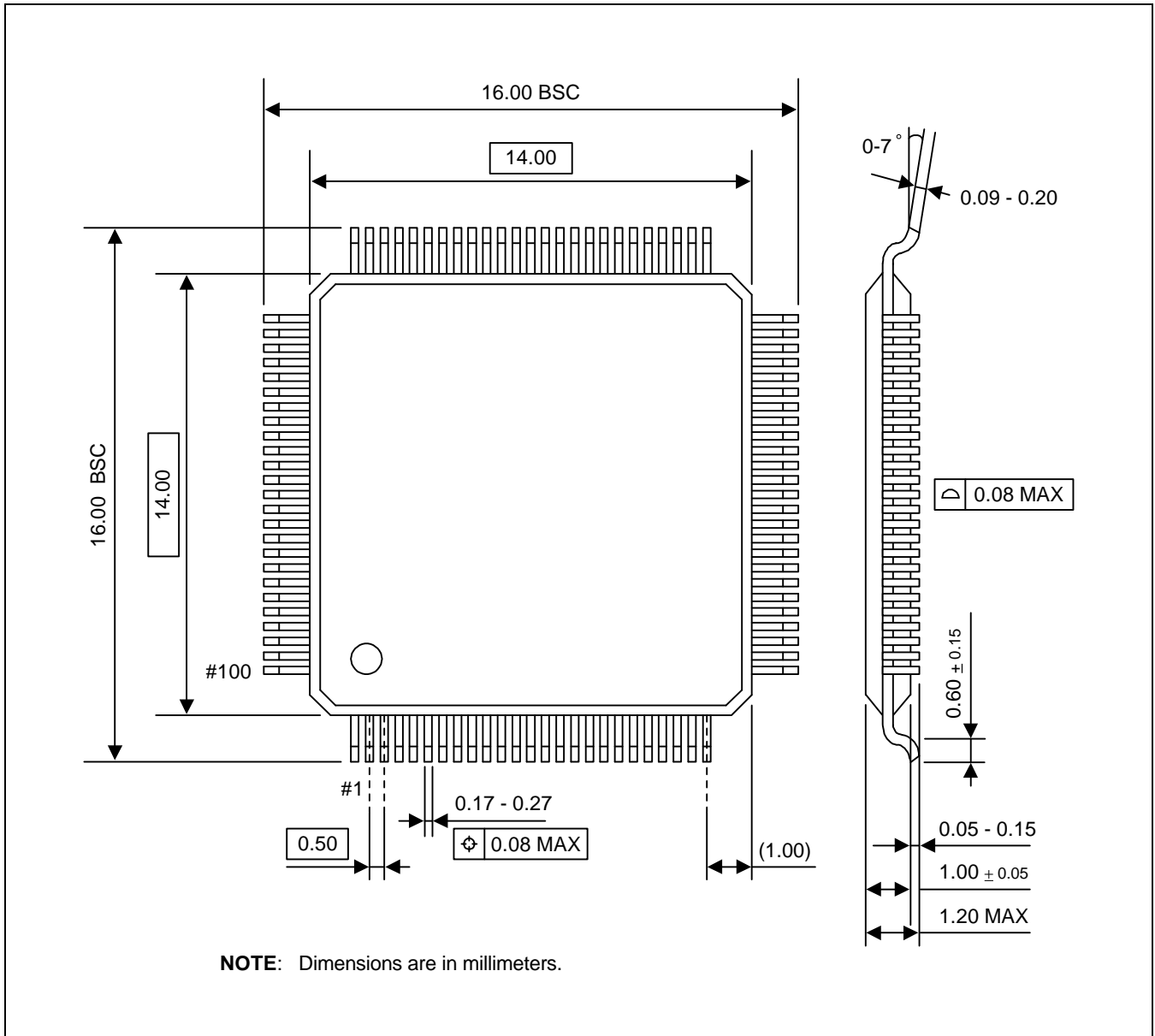
7.4.2 Display Output Timing Characteristics



Item	Symbol	Min	Typ	Max	Units
Propagation Delay Time from PCKO, Output RO0~7, GO0~7, BO0~7, PHSO, PVSO, PDEN	T_{PD}	- 3	0	3	ns
Frequency, Output Display Clock PCKO	F_D			100	MHz
Duty Cycle, Output Display Clock PCKO	C_{duty}	45	50	55	%
Rise Time, Output Display Clock PCKO	T_r			3	ns
Fall Time, Output Display Clock PCKO	T_f			3	ns

8 PACKAGE DIMENSION

8.1 100-TQFP-1414



9 FONTS

HP LaserJet 4ML PostScri							1/8
000H	001H	002H	003H	004H	005H	006H	007H
	1	2	3	4	5	6	7
008H	009H	00AH	00BH	00CH	00DH	00EH	00FH
8	9	A	B	C	D	E	F
010H	011H	012H	013H	014H	015H	016H	017H
G	H	I	J	K	L	M	N
018H	019H	01AH	01BH	01CH	01DH	01EH	01FH
O	P	Q	R	S	T	U	V
020H	021H	022H	023H	024H	025H	026H	027H
W	X	Y	Z			▣	▣
028H	029H	02AH	02BH	02CH	02DH	02EH	02FH
▣	▣	a	b	c	d	e	f
030H	031H	032H	033H	034H	035H	036H	037H
g	h	i	j	k	l	m	n
038H	039H	03AH	03BH	03CH	03DH	03EH	03FH
o	p	q	r	s	t	u	v

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HP LaserJet 4ML PostScri							2 / 8
040H 	041H 	042H 	043H 	044H 	045H 	046H 	047H
048H 	049H 	04AH 	04BH 	04CH 	04DH 	04EH 	04FH
050H 	051H 	052H 	053H 	054H 	055H 	056H 	057H
058H 	059H 	05AH 	05BH 	05CH 	05DH 	05EH 	05FH
060H 	061H 	062H 	063H 	064H 	065H 	066H 	067H
068H 	069H 	06AH 	06BH 	06CH 	06DH 	06EH 	06FH
070H 	071H 	072H 	073H 	074H 	075H 	076H 	077H
078H 	079H 	07AH 	07BH 	07CH 	07DH 	07EH 	07FH

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HP LaserJet 4ML PostScri							3 / 8
080H	081H	082H	083H	084H	085H	086H	087H
À	É	Ì	Ò	Ù	À	É	Ì
088H	089H	08AH	08BH	08CH	08DH	08EH	08FH
Ó	Ü	Ä	Ë	Î	Ò	Û	Ç
090H	091H	092H	093H	094H	095H	096H	097H
à	ë	ì	ò	ù	ä	è	î
098H	099H	09AH	09BH	09CH	09DH	09EH	09FH
ó	ü	ä	ë	î	ò	û	ç
0A0H	0A1H	0A2H	0A3H	0A4H	0A5H	0A6H	0A7H
À	É	Ì	Ò	Ù	À	Ö	Ñ
0A8H	0A9H	0AAH	0ABH	0ACH	0ADH	0AEH	0AFH
Ä	Š	Ž	Ÿ	Ɔ			
0B0H	0B1H	0B2H	0B3H	0B4H	0B5H	0B6H	0B7H
à	ë	ì	ò	ù	ä	ö	ñ
0B8H	0B9H	0BAH	0BBH	0BCH	0BDH	0BEH	0BFH
â	š	ž	ÿ	Ɔ			

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HP LaserJet 4ML PostScri							4 / 8
0C0H	0C1H	0C2H	0C3H	0C4H	0C5H	0C6H	0C7H
가	간	감	거	검	결	계	게
0C8H	0C9H	0CAH	0CBH	0CCH	0CDH	0CEH	0CFH
고	공	곽	국	기	깨	널	노
0D0H	0D1H	0D2H	0D3H	0D4H	0D5H	0D6H	0D7H
누	뉴	뉴	느	능	나	만	망
0D8H	0D9H	0DAH	0DBH	0DCH	0DDH	0DEH	0DFH
때	도	동	드	디	또	력	립
0E0H	0E1H	0E2H	0E3H	0E4H	0E5H	0E6H	0E7H
럿	레	름	르	름	리	막	미
0E8H	0E9H	0EAH	0EBH	0ECH	0EDH	0EEH	0EFH
매	면	명	모	미	반	방	방
0F0H	0F1H	0F2H	0F3H	0F4H	0F5H	0F6H	0F7H
벤	보	본	볼	부	분	블	비
0F8H	0F9H	0FAH	0FBH	0FCH	0FDH	0FEH	0FFH
사	삭	상	씩	선	설	성	세

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HP LaserJet 4ML PostScri							5 / 8
100H	101H	102H	103H	104H	105H	106H	107H
소	송	수	스	시	식	산	실
108H	109H	10AH	10BH	10CH	10DH	10EH	10FH
아	알	어	언	영	연	영	오
110H	111H	112H	113H	114H	115H	116H	117H
은	요	용	의	유	운	이	음
118H	119H	11AH	11BH	11CH	11DH	11EH	11FH
이	인	일	입	자	작	장	제
120H	121H	122H	123H	124H	125H	126H	127H
제	저	적	전	정	조	주	중
128H	129H	12AH	12BH	12CH	12DH	12EH	12FH
직	실	짐	정	제	조	주	죽
130H	131H	132H	133H	134H	135H	136H	137H
취	치	케	켜	크	키	타	익
138H	139H	13AH	13BH	13CH	13DH	13EH	13FH
테	투	파	평	하	한	할	해

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HP LaserJet 4ML PostScri							6 / 8
140H	141H	142H	143H	144H	145H	146H	147H
행	현	화	확	회	호	히	어
148H	149H	14AH	14BH	14CH	14DH	14EH	14FH
에	어	어	어	어	어	어	어
150H	151H	152H	153H	154H	155H	156H	157H
어	어	어	어	어	어	어	어
158H	159H	15AH	15BH	15CH	15DH	15EH	15FH
어	어	어	어	어	어	어	어
160H	161H	162H	163H	164H	165H	166H	167H
어	어	어	어	어	어	어	어
168H	169H	16AH	16BH	16CH	16DH	16EH	16FH
어	어	어	어	어	어	어	어
170H	171H	172H	173H	174H	175H	176H	177H
어	어	어	어	어	어	어	어
178H	179H	17AH	17BH	17CH	17DH	17EH	17FH
어	어	어	어	어	어	어	어

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HP LaserJet 4ML PostScri							7 / 8
180H	181H	182H	183H	184H	185H	186H	187H
188H	189H	18AH	18BH	18CH	18DH	18EH	18FH
190H	191H	192H	193H	194H	195H	196H	197H
198H	199H	19AH	19BH	19CH	19DH	19EH	19FH
1A0H	1A1H	1A2H	1A3H	1A4H	1A5H	1A6H	1A7H
1A8H	1A9H	1AAH	1ABH	1ACH	1ADH	1AEH	1AFH
1B0H	1B1H	1B2H	1B3H	1B4H	1B5H	1B6H	1B7H
1B8H	1B9H	1BAH	1BBH	1BCH	1BDH	1BEH	1BFH

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HP LaserJet 4ML PostScri								8 / 8
1C0H	1C1H	1C2H	1C3H	1C4H	1C5H	1C6H	1C7H	
1C8H	1C9H	1CAH	1CBH	1CCH	1CDH	1CEH	1CFH	
1D0H	1D1H	1D2H	1D3H	1D4H	1D5H	1D6H	1D7H	
1D8H	1D9H	1DAH	1DBH	1DCH	1DDH	1DEH	1DFH	
1E0H	1E1H	1E2H	1E3H	1E4H	1E5H	1E6H	1E7H	
1E8H	1E9H	1EAH	1EBH	1ECH	1EDH	1EEH	1EFH	
1F0H	1F1H	1F2H	1F3H	1F4H	1F5H	1F6H	1F7H	
1F8H	1F9H	1FAH	1FBH	1FCH	1FDH	1FEH	1FFH	

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